Design and Performance of the Silicon Pixel Detector Modules for the CMS Experiment

Dissertation

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Zusammenfassung

Der LHC Beschleuniger (Large Hadron Collider) ist ein ringförmiger Proton-Proton Beschleuniger, der zur Zeit am Europäischen Zentrum für Teilchenphysik (CERN) in Genf gebaut wird. Die Schwerpunktsenergie der kollidierenden Protonen wird 14 TeV sein, bei einer geplanten Luminosität von 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Die Datennahme soll im Herbst 2007 mit einem Probelauf bei einer niedrigeren Luminosität beginnen. Mit dem LHC wird es möglich sein, Teilchenphysik im Energiebereich von TeV zu betreiben. Das physikalische Meßprogramm umfaßt weitergehende Studien betreffend der Gültigkeitsgrenzen des Standard Modells (SM) und die Suche nach neuen physikalischen Erkenntnissen jenseits des SM. Den Schwerpunkt bildet jedoch die Entdeckung des Higgs Bosons. Viele Ereignisse werden b-Jets enthalten, die für die Identifikation der Zerfallskanäle mit top Quarks oder Higgs Bosonen dienen. Um die effiziente Erkennung dieser b-Jets zu ermöglichen, müssen die Flugbahnen der Zerfallsprodukte mit hoher Präzision bestimmt werden, um die Streuparameter zu ermitteln. Dafür müssen die innersten Lagen der Spurdetektoren so nah wie möglich am Wechselwirkungspunkt liegen, was eine hohe Strahlenbelastung bedeutet. Um Vielfachstreuung, die das räumliche Auflösungsvermögen verschlechtert, an den Detektorlagen zu vermeiden, muß die eingebaute Materialmenge minimal sein.

Der CMS (Compact Muon Solenoid) Detektor ist eines von den zwei großen Vielzweckexperimenten, die momentan am LHC aufgebaut werden. Die hohe Spurdichte im Bereich nahe des Wechselwirkungspunktes erfordert stark segmentierte Siliziumdetektoren, um die Spuren auflösen zu können und die Rate vernünftig niedrig zu halten. Die drei innersten Lagen des zentralen Spurdetektors, bestehend aus ungefähr 800 Modulen, und jeweils zwei Lagen in Vorwärtsrichtung, werden mit Silizium Pixeldetektoren ($\sim 66 \times 10^6$ Pixel) ausgestattet sein. Sie liefern 3-dimensionale Raumpunkte und tragen somit zu einer effizienten Spurrekonstruktion auch unter hohen Raten bei. Die Pixelgröße ist 100 µm $\times$ 150 µm ($r\phi \times z$) mit einer räumlichen Auflösung im Bereich von 15 µm. Sie hängt von der Bestrahlungsdosis und der Position im Pixeldetektor ab. Der Sensor und die Auslesechips (ROC = Readout Chip) bleiben voll funktionsfähig bis zu einer akkumulierten Strahlendosis von 6×10^{14} $\mathrm{n_{eq}/cm^2}$. Dies entspricht den ersten vier Jahren des LHC Betriebes für die innerste Detektorlage.

In dieser Arbeit sind der Aufbau und die Leistungsmerkmale der Module für den zentralen zylinderförmigen Teil des CMS Pixeldetektors einschließlich der Funktionsweise der Komponenten beschrieben.

Die Module bestehen aus 16 Auslesechips, deren Kanäle einzeln mit den 66560 Pixeln des Sensors, mittels einer eigens entwickelten Technik, verbunden sind. Spezielle Signal- und Stromkabel verbinden die Module mit der Steuer- und Ausleseelektronik. Auf dem Modul werden die Signale und die Spannungen von einer flexiblen, sehr leichten Leiterplatte zu den

ROCs verteilt. Diese Leiterplatte (HDI = High Density Interconnect) ist mit dem Token Bit Manager Chip (TBM) bestückt, der die Auslese des Moduls organisiert. Zur mechanischen Versteifung der Modulstruktur ist sie auf zwei Trägerstreifen geklebt. Insgesamt beläuft sich die Materialmenge eines Moduls auf 1.2 % einer Strahlungslänge, beziehungsweise 1.6 % einschließlich der mechanischen Struktur und der Kühlflüssigkeit. Die Konstruktion des Moduls wurde bestimmt durch die physikalischen Anforderungen sowie auch durch die extremen Betriebsbedingungen.

Der starke Strahlungsuntergrund verursacht nicht nur eine allmähliche Änderung der Charakteristik des Auslesechips, sondern korrumpiert auch die Ausleseelektronik. Eine Folge davon sind unkontrolliert veränderte Speicherzellen-Inhalte (SEU = Single Event Upsets), die ein ernstes Problem für den Betrieb des Pixeldetektors darstellen. Für die Untersuchung der SEU Problematik wurden Testschaltkreise mit Schieberegistern, bestehend aus Speicherzellen (SRAM = Static Random Access Memory) wie sie im ROC verwendet wurden, mit und ohne Schutzkapazität entwickelt und hergestellt. Der SEU Wirkungsquerschnitt der Teststrukturen und eines Auslesechips (ROC PSI46V1) wurden bei Strahltests bestimmt. Die gemessenen SEU Wirkungsquerschnitte für geschützte Speicherzellen sind 2.57×10^{-16} cm^2/SRAM für einen Übergang von 0→1 und 0.529×10^{-16} cm^2/SRAM für eine Änderung von 1→0. Die Verbesserung bedingt durch die Schutzkapazität beläuft sich mindestens auf einen Faktor 100 und hängt vom ursprünglich gespeicherten Zustand ab. Mit den gemessenen Wirkungsquerschnitten ergibt sich eine SEU Rate pro Kontrollnetzwerk für die innersten zwei Lagen von weniger als 0.03 Hz. Durchschnittlich wird es ungefähr 8 Stunden dauern, um 1‰ aller Speicherzellen, die von einem Kontrollnetzwerk bedient werden, zu korrumpieren. Dies ergibt ca. 1 SEU pro Sekunde für den gesamten zentralen Teil des Pixeldetektors ($\sim 48 \times 10^6$ Pixel). Deswegen kann auf ein wiederholtes Programmieren der Speicherzellen während der Datennahme höchstwahrscheinlich verzichtet werden.

Der Pixeldetektor muß permanent Daten nehmen und gleichzeitig ausgelesen werden können, um die Totzeit minimal zu halten und eine maximale Effizienz bei einer bestimmten globalen Komparatorschwelle zu erreichen. Um dies zu garantieren, muß das elektronische Übersprechen auf dem Modul so gering wie möglich sein. Das gemessene Übersprechen hängt von der Anzahl getroffener Pixel und dem Zustand des Auslesevorgangs ab. Für Protonkollisionen wurde eine Verschiebung der globalen Schwelle um ca. 200 Elektronen gemessen. Sogar für den Fall von Ionenkollisionen, mit der entsprechend höheren Anzahl von getroffenen Pixeln, ergibt sich eine Verschiebung der Schwelle von weniger als 300 Elektronen. Verglichen mit einer globalen Komparatorschwelle von 2500 Elektronen, die das Entwicklungsziel des Pixeldetektors ist, ist das gemessene Übersprechen tolerabel.

Die Ineffizienz des Pixeldetektors muß über den gesamten Spurdichtenbereich, der unter LHC ähnlichen Bedingungen erwartet wird, minimal sein. Um dies zu testen, wurde ein Pixeldetektor Modul zum ersten mal unter LHC ähnlichen Bedingungen in einem hoch-raten Pionenstrahl betrieben. Das Zusammenspiel zwischen dem TBM und den 16 ROCs funktionierte problemlos. Die gemessene Ineffizienz konnte mit der auf den Strahltest angepaßten Simulation reproduziert werden. Daher scheinen die Datenverluste in der Simulation korrekt berücksichtigt zu sein. Auf reale CMS Bedingungen angewandt, ergibt sie eine Ineffizienz von 3.8 % für die innerste Lage bei einer Triggerrate von 100 kHz. Die niedrigste globale Komparatorschwelle für einen stabilen Betrieb des Moduls im Strahltest war 2000 Elektronen.

Da die Leistungscharakteristik der Module die Anforderungen erfüllt, hat die Serienproduktion mit dem in dieser Arbeit beschriebenen Aufbau der Module bereits begonnen. Das angestrebte Ziel der Produktion sind 4 Module pro Tag. Nachdem ungefähr 400 Module für die 4 cm und die 7 cm Lage hergestellt sein werden und die Inbetriebnahme des zentralen Teils des Pixeldetektors erfolgt ist, werden die ersten Messungen Ende 2007 beginnen.

Abstract

The Large Hadron Collider (LHC) is a circular proton-proton collider currently under construction at the European Organization for Nuclear Research (CERN) in Geneva. The center-of-mass energy will be 14 TeV with a design luminosity of 10^{34} cm^{-2}s^{-1}. The scheduled start-up for taking data with a low luminosity pilot run is late 2007. The LHC will allow to explore new physics at the TeV scale with a physics program including investigations of the limits of the Standard Model (SM) and the search for physics beyond the SM. The focus lays on the search for the Higgs boson. Many interesting events contain b-jets which will be used to identify physics channels with top quarks or the Higgs boson. In order to allow an efficient recognition of these b-jets, trajectories of the reaction products have to be measured with high precision to determine the impact parameter. Therefore the tracking has to extend as closely as possible towards the interaction point. This results also in a high integrated radiation dose for the innermost layer. To reduce multiple scattering effects which downgrade the spatial resolution the amount of material must be minimal.

The Compact Muon Solenoid (CMS) detector is one of the two large multi purpose experiments which are being installed at the LHC. The high track density in the region close to the interaction point requires highly segmented silicon detectors to separate the tracks and to keep the occupancy low. The three innermost tracking layers composed of about 800 modules and two sets of forward disks will be equipped with hybrid silicon pixel detectors ($\sim 66 \times 10^6$ pixels). They provide true 3-dimensional space point information and will contribute to an efficient track reconstruction even under high rate conditions. The pixel size is 100 µm $\times$ 150 µm ($r\phi \times z$) and the spatial resolution is in the range of 15 µm depending on the irradiation fluence and the position in the pixel detector. The sensor and the readout chips remain fully operational until 6×10^{14} n$_{\mathrm{eq}}$/cm^2 corresponding to the first four years of LHC operation for the innermost layer.

In this thesis the design and the performance of the modules for the barrel of the CMS pixel detector including the functionality of their components is described.

The modules are composed of 16 Readout Chips (ROCs) connected to the sensor segmented into 66560 pixels by a dedicated bump bonding technique. The control signals and the power are supplied to the module by the control cable and the power cable. On the module the signals and the power are distributed to the ROCs by a flexible, low mass printed circuit board. This High Density Interconnect (HDI) is equipped with the Token Bit Manager (TBM) chip which organizes the readout of the module. For the mechanical fixation the sandwich structure is glued to the base stripes. In total the amount of material sums up to about 1.2 % of a radiation length and to 1.6 % including the support structure and the coolant. The design of the module components was directed by the physics requirements, but

also by the challenging operating conditions.

The harsh radiation environment causes not only a gradually change in the characteristic of the ROC but also Single Event Upsets (SEUs). The consequence of SEUs are instantaneously corrupted memory cells which are a serious operational problem for the pixel detector. For investigating the SEU problem test structures with shift registers consisting of Static Random Access Memory (SRAM) cells as used in the ROC with and without a protection capacitor were designed. The SEU cross sections of the SRAM cells and of a pixel readout chip (ROC PSI46V1) were determined in a beam test. The measured SEU cross sections for the protected storage cells are 2.57×10^{-16} cm^2/SRAM for a transition from 0→1 and 0.529×10^{-16} cm^2/SRAM for a changeover from 1→0. The benefit of the protection capacitor is at least about a factor of 100 in the cross section and depends on the switching direction. With the measured cross sections the SEU rate per control network for the first and second layer is less than 0.03 Hz. In average it will take about 8 hours to switch 1‰ of all SRAM cells controlled by the corresponding digital optical link. This yields in about 1 SEU per second for the entire pixel detector barrel ($\sim 48 \times 10^6$ pixels). Therefore reloading single pixel cells during the data taking period can be most likely avoided.

The pixel detector has to perform continuous data taking and simultaneous readout operation with minimal dead-time to achieve a maximum efficiency at a certain global threshold. To guaranty this the electronic crosstalk on the module must be as low as possible. The measured crosstalk depends on the cluster size and the states of the readout. For proton collisions the measured threshold shift is about 200 electrons. Even in the case of heavy ion collisions with the corresponding larger cluster sizes the threshold shift is smaller than 300 electrons. Compared to the global threshold of 2500 electrons which is the design goal of the pixel vertex detector the measured pickup is tolerable.

The detection inefficiency of the pixel detector must be minimal up to the expected track densities under LHC like conditions. To test the performance a pixel detector module was operated the first time under LHC like conditions in a high rate pion beam. No operational problem in the interaction of the 16 ROCs with the TBM was observed. The measured inefficiency could be reproduced with the simulation adapted to the beam test. The data losses seems to be described correctly in the simulation and applied to real CMS conditions an inefficiency of 3.8 % for the innermost layer and a level-1 trigger rate of 100 kHz is expected. The lowest global comparator threshold for a stable module operation in the beam test was about 2000 electrons.

Since the module performance fulfill the requirements the mass production of the modules has already started with the final design described in this work. The goal of the production is to assembly 4 modules per day. After the production of about 400 modules for the 4 cm and 7 cm layer and the successful commissioning of the barrel part of the pixel vertex detector, the first data-taking is expected for late 2007.

Contents

Chapter 1

Introduction

The Large Hadron Collider (LHC) is a circular proton-proton collider with a center-of-mass energy of 14 TeV. The design luminosity is 10^{34} $cm^{-2}s^{-1}$. The Compact Muon Solenoid (CMS) detector is one of the two large multi purpose experiments which are currently being installed at the LHC. It is planned to start taking data for late 2007. The LHC will allow to explore new physics at the TeV scale. Its physics program includes investigations of the limits of the Standard Model (SM) and the search for physics beyond the SM. The focus lays on the search for the Higgs boson.

In Chapter 2 the LHC and the CMS detector are presented. The CMS pixel vertex detector has to provide true space point information for the impact parameter determination and the vertex reconstruction with high precision. The design of the pixel detector is described. Especially the challenging requirements with respect to the physics program are derived.

The basic building block of the barrel part of the pixel vertex detector is a module. In Chapter 3 the design of the module is specified. The module is composed of the 16 Readout Chips (ROCs), the sensor, the High Density Interconnect (HDI) with the Token Bit Manager (TBM) chip, the signal cable, the power cable and the base stripes. These components are explained in detail.

The functionality of the ROC is described in Chapter 4. The functional blocks of the ROC are the sensitive pixel array, the double column periphery and the global part. The performance of the analog readout is shown and the measurements concerning the degradation of the performance after irradiation are presented. The leakage current tolerance of the preamplifier is investigated.

Chapter 5 is dedicated to Single Event Upset (SEU) investigations. The basic mechanisms for the generation of SEUs is shown. Test structures with unprotected and protected memory cells were designed. The SEU cross sections were determined with the test structures and a precursor version of the ROC in a beam test. The results are presented and the consequences of the resulting SEU rates for the ROC and the pixel detector control system are drawn.

In Chapter 6 the laboratory measurements with prototype modules are described in detail. The results of the intra module crosstalk investigations are shown for various phases of the module readout. The timing of the token passage on the module and measurements concerning the analog readout chain of the pixel detector are presented.

A final module was operated in a high rate beam test under LHC like conditions. The test setup consisting of a beam telescope for the track reconstruction and the test module

is described in Chapter 7. The focus in the beam test was on investigating the efficiency in dependence of e.g. the track density, the latency and the trigger rate. The measured inefficiencies are compared with the data loss results of simulations and discussed in detail.

Chapter 8 summarizes the most important results from this work and concludes with a short outlook.

Chapter 2

LHC and CMS

2.1 Large Hadron Collider at CERN

The Large Hadron Collider (LHC) is a new accelerator facility at the European Organization for Nuclear Research (CERN) in Geneva, Switzerland [1]. The LHC is a circular collider which collides 7 TeV protons on 7 TeV protons. A center-of-mass energy of 14 TeV will be available for the possible production of new heavy particles. In heavy ion ($^{208}Pb^{82+}$) collisions the center-of-mass energy will be 1148 TeV, i.e. 2.76 GeV per nucleon. The LHC accelerator is being built in the already existing Large Electron Positron (LEP) tunnel, which has a circumference of about 27 km (diameter 8.6 km). The commissioning of the LHC machine with beams is expected to start in the second half of 2007, followed by a low luminosity pilot physics run. To avoid the synchrotron radiation problem, which has been the limiting factor for the center-of-mass energy of the LEP collider, there are two possibilities: one could increase the radius of the collider (optimally reaching a linear collider) or one could increase the mass of the accelerated particles. This can be seen from the formula for synchrotron radiation loss for highly relativistic particles [2]:

$$-\Delta E = \frac{4\pi\alpha}{3R}\beta^3\gamma^4 \qquad \text{with} \qquad \beta = \frac{v}{c} \approx 1 \qquad \text{and} \qquad \gamma = \frac{E}{mc^2}, \tag{2.1}$$

with R being the radius of the accelerator, E the energy of the particles, m its mass and α is the fine structure constant. For financial reasons, the existing LEP tunnel was recycled to build a proton-proton collider. Since protons are about 2000 times heavier than electrons, the energy loss is $2000^4 \approx 10^{13}$ smaller than for electrons in the same tunnel with the same radius R. The maximum energy of a proton beam in the LEP tunnel is then determined by the maximum magnetic dipole field that can be achieved to provide the centripetal force for deflecting the particles[1]:

$$E\ [\text{TeV}] \approx 0.84 \times B\ [\text{Tesla}] \tag{2.2}$$

From the particle physics point of view (Sect. 2.2) there are solid theoretical arguments to assume that the mass scale of new physics phenomena will be around 1 TeV. An additional

[1] Derivation of E [TeV] $\approx 0.84 \times B$ [Tesla] (eq. 2.2): $p = e|B|r$ with $r = \frac{n_{dipole} \times l_{dipole}}{2\pi}$. $n_{dipole} = 1232$ is the number of bending dipole magnets in the LHC ring, $l_{dipole} = 14.3$ m is the length of the dipole magnets and the speed of light 3×10^8 m/s as an conversion factor from SI units to TeV.

complication at proton colliders is that protons are not elementary particles but composite objects, and the quarks and gluons inside the protons only carry a fraction of the proton momentum. Therefore, in order to be able to produce a statistically significant sample of e.g. 1 TeV Higgs bosons, the *pp* center-of-mass energy of the collider should be in the multi TeV range. For the LHC project superconducting dipole magnets with 8.33 T nominal magnetic field are used which, according to eq. 2.2, corresponds to a beam energy of 7 TeV, i.e. 14 TeV *pp* center-of-mass energy. Since LHC collides two beams with particles of equal charge, two beam pipes with opposite magnetic field configurations are necessary. This has been achieved in the design of the LHC dipole magnets.

In four intersection regions along the underground LHC tunnel, the particle bunches will collide. Around the collision points, huge detectors will be built in order to measure with high precision and efficiency the properties of the particles that are produced in the collisions. The event rate R at which a certain type of physics events are produced by a collider is given by

$$R = \mathcal{L}\sigma \tag{2.3}$$

where σ is the cross section of the physics process under study and $\mathcal{L}$ is the luminosity of the collider. In order to keep the same statistical significance, an increase of the energy of a collider requires an increase in its luminosity proportional to E^2 since the cross section of parton-parton processes decreases with that amount ($\sigma \sim 1/E^2$). In fact, for a hadron collider, the situation is more complicated since one has to take into account the structure functions[2] which drop steeply with increasing x. These considerations lead to a design luminosity of 10^{34} cm^{-2}s^{-1} ("high luminosity"). The first few years LHC will run at a reduced luminosity of 2×10^{33} cm^{-2}s^{-1} ("low luminosity"). The luminosity of an accelerator which collides bunches containing n_1 and n_2 particles at a bunch crossing frequency of f is given by

$$\mathcal{L} = f\frac{n_1 n_2}{4\pi\sigma_x\sigma_y} \tag{2.4}$$

where σ_x and σ_y characterize the Gaussian transverse beam profiles at the interaction point. Reaching the LHC design luminosity requires a small transverse beam profile, a high bunch collision frequency and a large number of particles per bunch. The nominal number of protons per bunch at LHC will be 10^{11}. Because of this large number, the average number of inelastic *pp* collisions ("minimum bias" events) per bunch crossing is high. Up to 20 minimum bias events for the design luminosity[3] are expected. This leads to very difficult experimental conditions, since the rare interesting events that may occur are superimposed ("piled-up") on top of these 20 minimum bias events. This implies that around 1000 charged particles

[2] The structure function gives the probability, that a parton (quark, antiquark or gluon) carries a momentum fraction between x and $x+dx$ of the nucleon momentum [3].

[3] Event rate R estimation with $\mathcal{L} = f\frac{n_1 n_2}{4\pi\sigma_x\sigma_y}$ (eq. 2.4) and $R = \mathcal{L}\sigma$ (eq. 2.3):

$$\sigma_x \approx \sigma_y \approx 16.7\ \mu\text{m}, n_1 \approx n_2 \approx 1.15 \times 10^{11}, f = 40\ \text{MHz} \Rightarrow \mathcal{L} \approx 1.5 \times 10^{34}\ \text{cm}^{-2}\ \text{s}^{-1}$$

$$\sigma_{pp\_inelastic} \approx 60\ \text{mb} \Rightarrow R = \mathcal{L} \times \sigma_{pp} \approx 900 \times 10^6\ \text{s}^{-1}$$

$$\text{No. minimum bias events} = R/f \Rightarrow \approx 23 \text{ minimum bias events/bunch crossing}$$

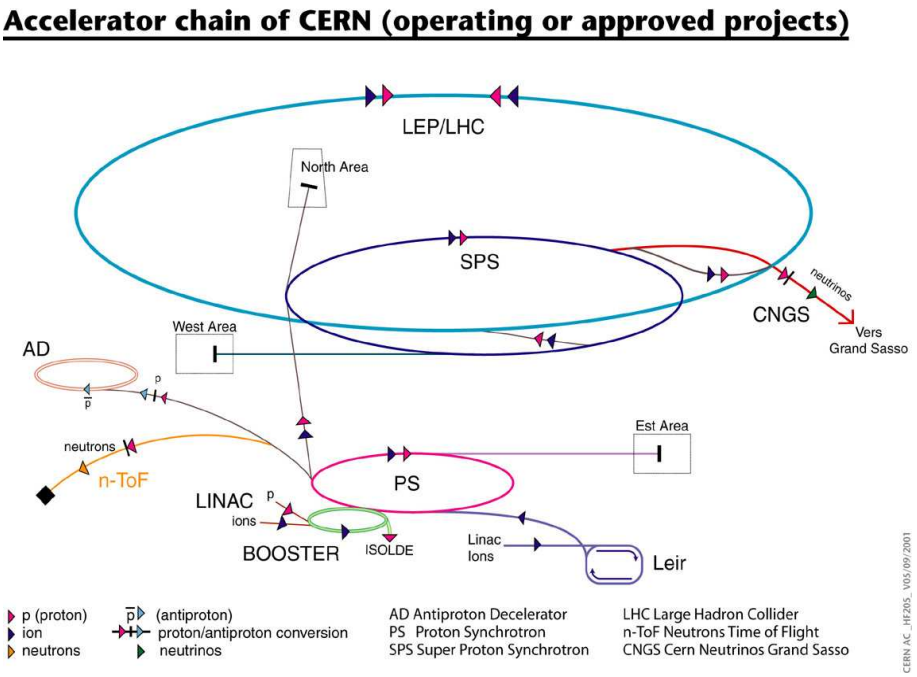

Figure 2.1: Chain of the accelerators at CERN.

will emerge from the interaction region for every bunch crossing. To keep the number of pile-up events low at a given luminosity, one has to use high granularity detectors with good time resolution. In addition the system has to operate at a high bunch crossing frequency. The bunch crossing frequency will be 40 MHz (every 25 ns a bunch crossing). Such a high frequency, however, imposes stringent requirements on the response time of the LHC detectors.

Contrary to most hadron colliders in the past, the LHC will produce pp collisions instead of the more traditional $p\bar{p}$ collisions. It is very difficult to produce sufficient amounts of antiprotons needed to achieve the LHC design luminosity in any case. Since at LHC energies the most active components of the protons in the production of new particles are the gluons rather than the quarks (and the distribution of gluons in protons and antiprotons is the same), pp collisions are equivalent to $p\bar{p}$ interactions. The protons are delivered to the LHC by an injector chain, composed of presently existing CERN accelerators. These accelerators have to be upgraded to meet the requirements of LHC in terms of intensity and number of bunches. The injection chain starts with the Linear Accelerator (LINAC) accelerating protons to an energy of 50 MeV. The particles are then injected into the Proton Synchrotron Booster (PSB) and later into the Proton Synchrotron (PS). The PS accelerates the protons to an energy of 26 GeV and forms the bunches with the correct 25 ns bunch structure. The last part of the injector chain is the Super Proton Synchrotron (SPS), which accelerates the protons up to an energy of 450 GeV and injects them into the LHC ring. The chain of accelerators is shown in Figure 2.1. To fill both LHC rings, 24 SPS cycles are needed. Taking into account the rise and fall time of several kicker magnets, the number of filled bunches in one LHC ring will be 2808 out of 3564. Assuming that the machine can be operated during about 200 days a year, the total integrated luminosity will be in the range of 10-35 fb^{-1} for the low luminosity phase

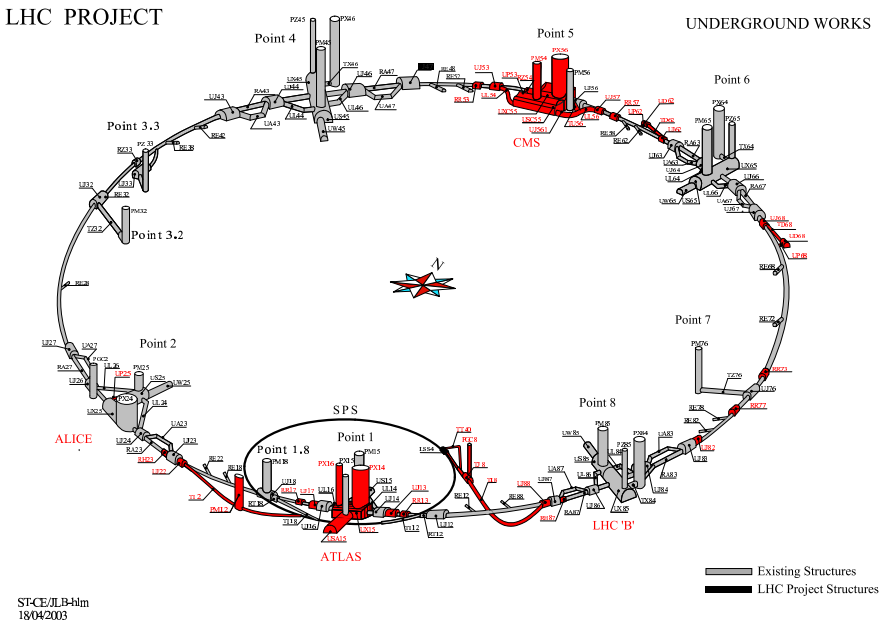

Figure 2.2: Overview of the LHC tunnel with the detectors and infrastructure.

and about 100-300 fb^{-1} for high luminosity period. During the startup of LHC the integrated luminosity will be limited by the time taken to start up LHC operation. The integrated luminosity is likely to be about 5 fb^{-1} in the first year [4].

At the four interaction regions with the colliding LHC beams, four experiments are in preparation. Two of them are general purpose detectors, the CMS (Compact Muon Solenoid) [5] and the ATLAS detectors (A Toroidal LHC ApparatuS) [6]. The third experiment, LHCb [7], will be specifically dedicated to b-physics studies. CMS, ATLAS and LHCb are designed for the operation in the proton-proton collision mode. The fourth detector, ALICE (A Large Ion Collider Experiment) [8], is specialized on heavy ion physics, beside the CMS and ATLAS heavy ion programs. In addition there is the TOTEM experiment [9], which will measure the total pp cross section and study elastic low-angle scattering at the LHC. Parts of TOTEM are located very close to CMS and other parts are positioned further downstream (150-220 m). The geographical location of all detectors in the LHC tunnel shows Figure 2.2. The LHC parameters relevant for the experiments are given in Table 2.1 [10].

2.2 Physics at the Large Hadron Collider

The main goal of the physics program of the two general purpose experiments is the exploration of the Standard Model (SM) limits: the search for SM and Supersymmetric (SUSY) Higgs bosons as well as searching for SUSY partners of the SM particles. Furthermore there is a b-physics program at LHC which will be mainly carried out at low luminosity running due to the need for low trigger thresholds and to avoid too many overlapping events. For the heavy ion program, the proton beams in the LHC accelerator will be replaced by ion beams. In

Proton energy at injection	450 GeV
Proton energy at collision	7 TeV
Dipole field at 7 TeV	8.33 T
Design Luminosity	1.0×10^{34} cm^{-2}s^{-1}
Bunch separation	25 ns
No. of bunches	2808
No. of particles per bunch	1.15×10^{11}
Circulating current per beam	0.582 A
Stored beam energy at collision	362 MJ
Energy loss per turn due to synchrotron radiation	6.71 keV
Luminosity lifetime	29.1 hr
Total pp cross section	100 mb
Inelastic pp cross section	60 mb
Number of events per bunch crossing	≈ 20
Beam crossing angle for CMS	285 µrad

Table 2.1: The Large Hadron Collider parameters relevant for the experiments at high luminosity mode.

Pb-Pb collisions, the nucleon-nucleon center-of-mass energy reaches 5.5 TeV, which is significantly higher than what is obtained at the currently working heavy ion colliders (e.g. RHIC: $\sqrt{s_{NN}} = 200$ GeV [11]). LHC will provide the opportunity to explore the quark-gluon plasma at very high energies.

Since CMS is dedicated to searches of SM and SUSY Higgs bosons, the focus lays in the following paragraphs on these parts of the physics program. Exemplary for the b-physics program the B_s^0-$\bar{B}_s^0$ system is taken (see Sect. 2.4.4) to derive the required spatial resolution for the pixel vertex detector.

2.2.1 Higgs Boson

The production cross section for the Higgs boson in pp collisions varies by many orders of magnitude (Fig. 2.3) and depends on the mass of the Higgs particle and the production mechanism. The dominant production channel is the gluon fusion. The next production channel over the whole mass range is the Vector Boson Fusion (VBF). Less important in terms of absolute cross section values are the associated productions ($t\bar{t}H$, HW), but they provide distinctive signatures. These can be relevant for largely background dominated decay channels ($b\bar{b}$, $\gamma\gamma$). The current lower limit on the Higgs mass from LEP is 114.4 GeV/c^2 [12] and a mass higher than 1 TeV/c is theoretically forbidden. Depending on the Higgs mass, different decay channels can be used for discovery (Fig. 2.5). In the mass range up to 130 MeV/c, the branching fractions (Fig. 2.6) of the Higgs boson are dominated by hadronic decays, which are difficult for the Higgs discovery at the LHC due to the large QCD backgrounds and the insufficient mass resolution that is obtainable for jets. $H \to b\bar{b}$ in $t\bar{t}$ is only useful for Higgs discovery in spite of the QCD $b\bar{b}$ background, because of the four b-jets in the decay channel

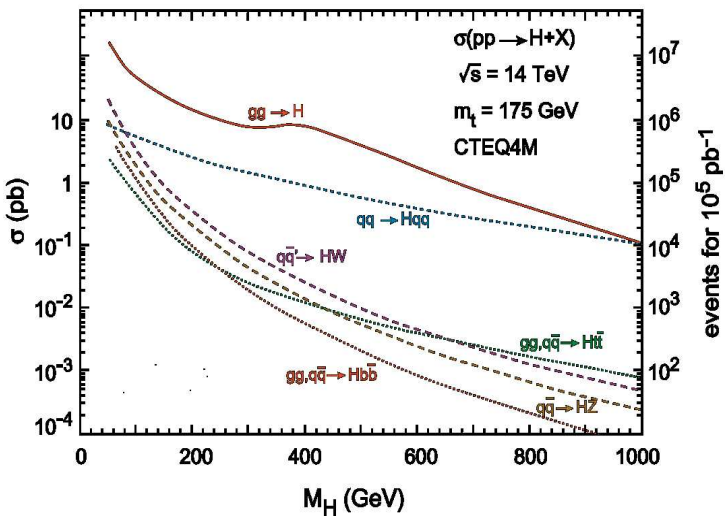

Figure 2.3: Cross sections for production of Standard Model Higgs Bosons and the number of events for an integrated luminosity of 100 fb^{-1} as a function of the Higgs mass.

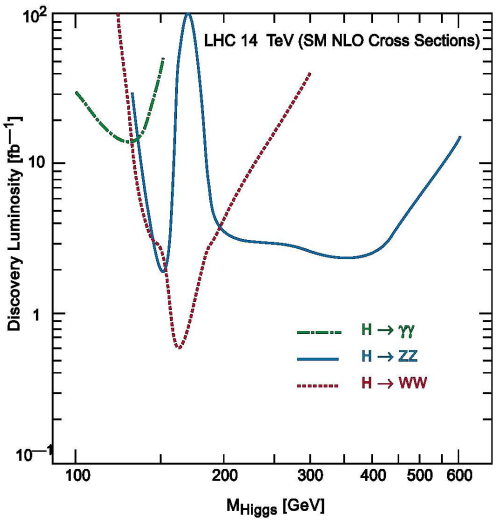

Figure 2.4: Standard Model Higgs discovery luminosity at LHC (one year high luminosity operation corresponds to about 100 fb^{-1}).

Mass range	Decay channel
100 GeV $\lesssim m_H \lesssim$ 150 GeV	$H \to \gamma\gamma$
90 GeV $\lesssim m_H \lesssim$ 120 GeV	$H \to bb$ in $t\bar{t}H$
130 GeV $\lesssim m_H \lesssim$ 200 GeV	$H \to ZZ^\star \to 4\ell (e or \mu)$
140 GeV $\lesssim m_H \lesssim$ 180 GeV	$H \to WW \to \ell\nu\ell\nu$
200 GeV $\lesssim m_H \lesssim$ 750 GeV	$H \to ZZ \to 4\ell$
500 GeV $\lesssim m_H \lesssim$ 1 TeV	$H \to 2\ell 2\nu$
$m_H \approx$ 1 TeV	$H \to WW \to \ell\nu + 2jets$
$m_H \approx$ 1 TeV	$H \to ZZ \to 2\ell + 2jets$

Figure 2.5: Experimentally accessible Higgs decay channels as a function of their mass [13].

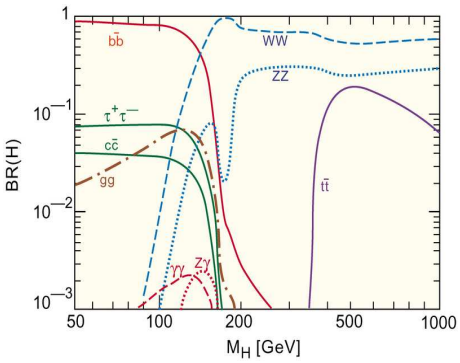

Figure 2.6: Branching ratios of Standard Model Higgs.

($H \to \ell\nu bjj\bar{b}\bar{b}$). The crucial detector related issues are the b-tagging, performed by the pixel detector and the jet energy determination. A very clear signal provides the channel $H \to \gamma\gamma$, but the Branching Ratio (BR) is smaller. The detection of this channel is performed by the Electro-magnetic Calorimeter (ECAL), which has been optimized for this search. The four lepton decay channels of the SM Higgs ($H \to ZZ^{(\star)} \to 4\ell$ and $H \to WW \to \ell\nu\ell\nu$ (e or μ)) can be used over a large mass range for discovery of the Higgs boson. The detection relies on the performance of the muon chambers, the tracker and the ECAL. Since the production cross section falls with rising Higgs mass, one has to use channels with larger branching ratios for the higher mass range. The event signatures include leptons, jets and missing transverse energy (E_T^{miss}) in the case of escaping neutrinos. For the E_T^{miss} determination the hadronic calorimeter performance is very important. The Higgs mass range up to approximately 1 TeV can be exploited with these channels.

At LHC the SM Higgs boson can be found over the entire expected range from the LEP limit to approximately 1 TeV. Three Higgs decay channels essentially cover the complete mass range: the two-photon channel for relatively light Higgs masses and WW and ZZ decays (with their subsequent leptonic decays) for higher masses. After one year of running LHC at high luminosity the discovery luminosity for various decay channels is achieved. In Figure 2.4 the discovery luminosity as a function of the Higgs mass is shown for the experimentally accessible decay channels. It varies for different channels between 1 and 100 fb^{-1}.

2.2.2 Supersymmetry

Supersymmetry requires a new particle spectrum. To determine the masses, couplings and decay chains of these new particles many parameters are needed. There are models that restrict the number of parameters. The most popular are the Minimal Supersymmetric Standard Model (MSSM). The MSSM has bosonic superpartners (sparticles) for the SM fermions - squarks ($\widetilde{q}$) and sleptons $\widetilde{\ell}$ - and fermionic partners for the SM bosons - gluinos ($\widetilde{g}$), neutralinos $\widetilde{\chi}^0_{1,2,3,4}$ and charginos ($\widetilde{\chi}^\pm_{1,2}$); neutralinos and charginos are commonly referred to as gauginos. There are also at least five Higgs bosons - two neutral scalars (h and H), one neutral pseudoscalar (A) and two charged ones ($H^\pm$).

The decays of supersymmetric particles, such as squarks and gluinos, involve cascades resulting in an abundance of leptons and jets (particularly b-jets and/or τ-jets). The following decay channels can be treated in a similar way as those for the SM Higgs:

- $h/A \to \gamma\gamma$
- $H \to ZZ^\star$
- $t\bar{t}h$ with $h \to b\bar{b}$

In addition there are the supersymmetric decay channels:

- $H/A \to \tau\tau, \mu\mu$
- $H/A \to hh$
- $A \to Zh$
- $A \to t\bar{t}$
- $H^\pm \to \tau\nu, t\bar{b}$
- $H/A \to sparticles$

Depending on the decay modes the detection of the decay products is performed with the various subdetectors of CMS. However, for the background rejection b-tagging for determination of the secondary vertices and the impact parameter are required. Therefore the pixel vertex detector will be crucial.

2.3 Compact Muon Solenoid Experiment

2.3.1 Summary of Detector Requirements

From a conceptual point of view, a general purpose collider detector should be designed as a perfect sphere around the collision point to detect all particles produced in the collision. Mechanically such a design would be extremely difficult and therefore a cylindrical shape has been adopted, essentially driven by the solenoidal magnet shape, still allowing for an almost

4π coverage. Modern collider detectors are composed of several subdetectors, arranged in concentric layers around each other and each of them dedicated to different and complementary types of measurements [15]. The requirements for the CMS detector to fulfill the demands of the LHC physics program (Sect. 2.2) can be summarized as follows [10]:

- Good muon identification and momentum resolution over a wide range of momenta in the region $|\eta|$ <2.5, good dimuon mass resolution and the ability to determine unambiguously the charge of muons[4].
- Good charged particle momentum resolution and reconstruction efficiency in the inner tracker. Efficient triggering and offline tagging of $\tau's$ and b-jets, requiring pixel detectors close to the interaction region.
- Good electromagnetic energy resolution, good diphoton and dielectron mass resolution, wide geometric coverage ($|\eta|$ <2.5), measurement of the direction of photons and correct localization of the primary interaction vertex, π^0 rejection and efficient photon and lepton isolation at high luminosities.
- Good E_T^{miss} and dijet mass resolution, requiring a hadron calorimeter with a large hermetic geometric coverage ($|\eta|$ <5) and with fine lateral segmentation.
- A financially affordable detector.

The following example should clarify, that in spite of the large number of minimal bias events a high efficiency is crucial for the detector. For a certain physics process, e.g. $H(1\,\mathrm{TeV}) \rightarrow ZZ \rightarrow 4\,\ell$ (Sect. 2.2), the production cross section for the generation of the 1 TeV Higgs bosons is in the range of 0.1 pb (Fig. 2.3). The branching ratio for the decay of the Higgs into ZZ is about 30 % (Fig. 2.6) and for $Z \rightarrow \mu\mu$ is about 3 %. This gives using equation 2.3 about 10 events per year for all lepton flavors, which makes an extremely high efficiency of the detector necessary. The particular interest on muons originates from the fact that muons are particles with a large penetrating power which makes them very suitable for experimental observation. This means that efficient detection and precise reconstruction even at high luminosities is crucial. Muons are also important signatures for many types of new physics that CMS wants to discover or study (Sect. 2.2). These arguments justify the priority that CMS has given to muon detection. Accounting for the large multiplicity of charged particles in the hadron collisions with high luminosity, the detector has to be granular enough to minimize the probability of piling up particles be in the same detector unit as interesting objects. In addition, the identification of the b-decays, which is equally important for Higgs, t- and b-physics, requires the reconstruction of secondary vertices with a very high spatial resolution.

2.3.2 CMS Subdetectors

The main features of the CMS detector are a high-field solenoid, a full silicon-based tracking system, and a fully active scintillating crystal-based electromagnetic calorimeter. The overall

[4]Pseudorapidity is defined as $\eta = -\ln\tan\frac{\Theta}{2}$, where Θ is the angle between the particle direction of flight and the beam pipe [3]. η is the appropriate parameter for pp colliders, since the number of particle tracks per unit of pseudorapidity is nearly constant (Fig. 2.11) [5].

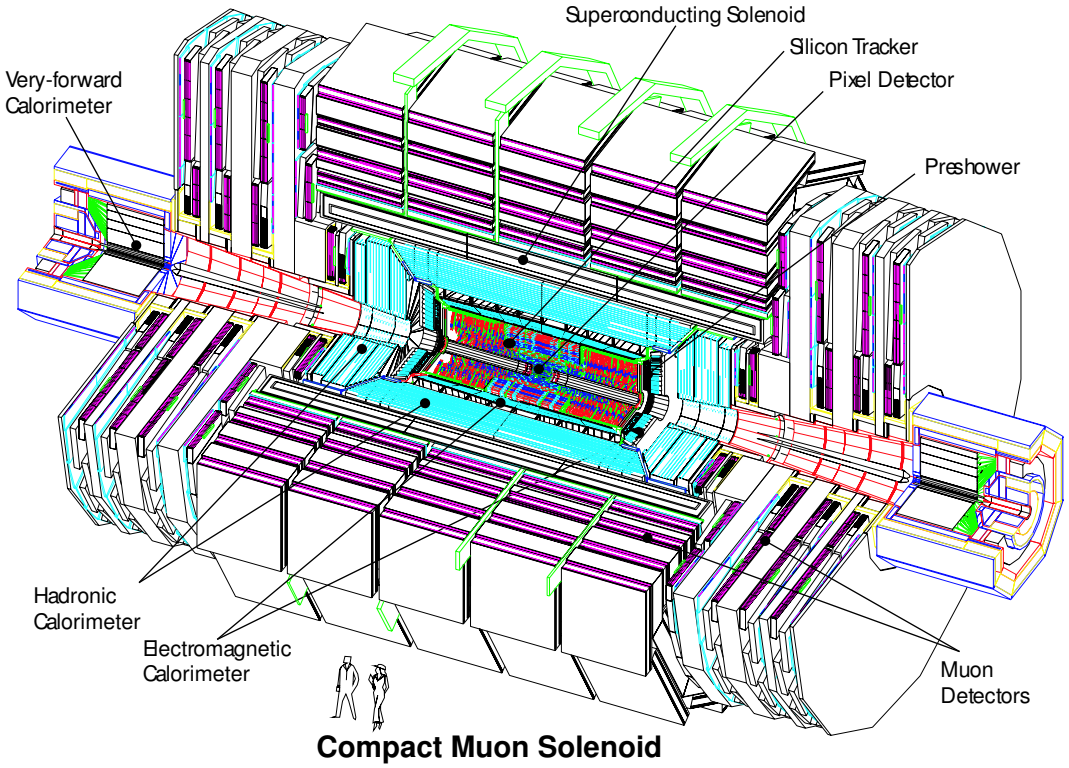

Figure 2.7: Exploded view of the CMS detector.

layout of CMS detector is shown in Figure 2.7[5]. A transverse cross section of the CMS detector can be seen in Figure 2.8. The tracks of charged and neutral particles in the various subdetectors are shown. Crucial to the detection and measurement of charged particles is the choice of the magnetic field configuration. A magnetic field along the beam axis deflects charged particles in the transverse plane. The precision of the muon momenta reconstruction depends on the strength of the magnetic field and the size of the detector. This can be understood by means of the following equation, which describes the moving of a charged particle in a magnetic field (eq. 2.2):

$$p_T \text{ [GeV/c]} = 0.3 \times B \text{ [Tesla]} \; r \text{ [m]} \tag{2.5}$$

where p_T is the transverse momentum of the particle in GeV/c, B is the magnetic field in Tesla and r is the bending radius in m. The factor 0.3 is a conversion factor from SI units to GeV/c. With the definitions in Figure 2.9 one has

$$\sin\frac{\theta}{2} \approx \frac{\theta}{2} \approx \frac{L}{2r} \approx \frac{0.3BL}{2p_T} \tag{2.6}$$

[5]The coordinate frame adopted to CMS has its origin centered at the nominal collision point inside CMS. The x-axis points radially inwards toward the center of LHC and the y-axis points vertically upwards. Thus, the z-axis points along the beam direction toward the Jura mountains. The azimuthal angel ϕ is measured from x-axis in x-y-plane. The polar angel Θ is measured from the z-axis.

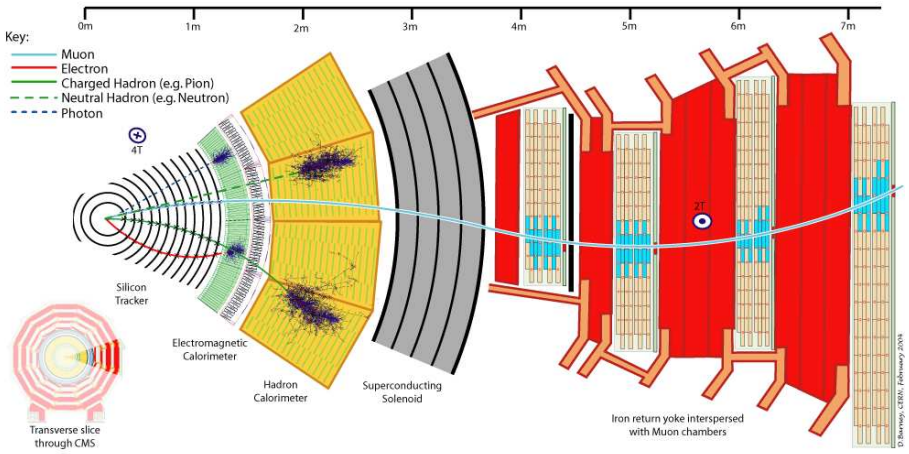

Figure 2.8: Transverse cross section of the CMS detector. The tracks of neutral and charged particles are shown.

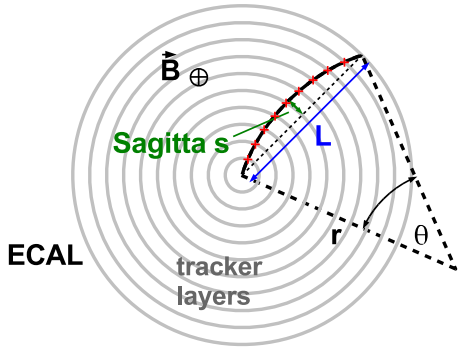

Figure 2.9: Transverse view of the deflection of a charged particle in the solenoidal magnetic field in the region of the tracker.

The actual quantity measured in the tracker is not the bending radius r but the sagitta s (Fig. 2.9), given by:

$$s = r - r\cos\frac{\theta}{2} \approx r\left(\frac{1}{2}\frac{\theta^2}{4}\right) \approx \frac{r\theta}{8}\frac{0.3BL}{p_T} \approx \frac{0.3BL^2}{8p_T}. \tag{2.7}$$

The relative error on the p_T measurement can be written as

$$\frac{\sigma_{p_T}}{p_T} = \frac{\sigma_s}{s} = \sigma_s\frac{8p_T}{0.3BL^2} \tag{2.8}$$

This equation does not include contributions from energy loss and multiple scattering. It has also no correction factors depending on the number and position of the measured points along the track. The simple result shows, that the precision on the momentum measurement of charged particles is proportional to $1/BL^2$. One aspect of this proportionality is, that e.g.

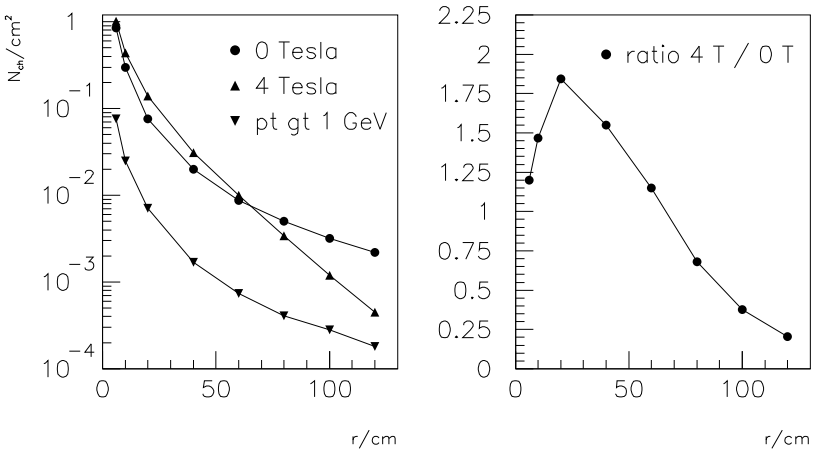

Figure 2.10: Charged particle density per cm^2 at $\eta = 0$ as a function of the distance from the interaction point for 20 minimum bias events superimposed.

by increasing the strength of the magnetic field and keeping the sagitta constant, the required L could be reduced. Under the assumption that the price for crystals for the Electro-magnetic Calorimeter (ECAL) is proportional to the volume, there will be a benefit with respect to the costs of the detector. A secondary effect of the magnetic field is the reduction of the occupancy of the ECAL channels. In the absence of the magnetic field the charged track density falls off as $1/r^2$. r is the radial distance from the collision point. The presence of the magnetic field modifies the charged particle density profile. Under the influence of the 4 Tesla magnetic field, the track density is up to a radius of about 65 cm increased and above this radius lower than without a magnetic field (Fig. 2.10). This has important implications for the architecture of the CMS detector [5], especially for the ECAL and the central tracker. CMS opted for a high magnetic field and a compact design of the detector while ATLAS has a large detector with moderate magnetic field.

2.3.2.1 Superconducting magnet

The starting point of the CMS detector design was the choice of the magnet system [16]. The superconducting solenoid with a length of 13 m and an inner diameter of 5.9 m creates a uniform field. The strength is 4 T in order to achieve a good momentum resolution within a compact spectrometer (eq. 2.8). The magnetic flux is returned through saturated iron yokes (return yokes) with a magnetic field of about 2 T. The return yokes are instrumented with four muon "stations" to ensure robustness and full geometric coverage. The inner width of the magnet coil is large enough to accommodate the calorimetry (ECAL and HCAL) and the central tracker inside.

2.3.2.2 Muon chambers

Muons are often present in the final state topologies of the physics, the LHC is designed to explore. For this reason the ability to trigger on and reconstruct muons at highest luminosities

is central to the concept of CMS (Sect. 2.2). Because of their long lifetime and high mass muons are a clean measurable object. Therefore precision measurements in the bending plane and along the beam are essential. This can be achieved by fine segmentation. For trigger reasons, the time resolution should be smaller than the bunch separation of 25 ns. The muon system is divided in a barrel part ($|\eta|$ <1.2) and two end caps (0.9< $|\eta|$ <2.4) [17]. The total thickness of the absorber before the last muon station amounts to 16 interaction lengths[6], allowing good muon identification. The muon system uses three different technologies to detect and measure the muons: drift tubes in the barrel region, cathode strip chambers in the end cap region, and Resistive Plate Chambers (RPC) in both the barrel and the end cap. The use of different technologies was chosen on the basis of the expected particle rates, the predominating magnetic fields and the required resolution at various $|\eta|$ regions. The RPCs deliver a fast, highly segmented signal for the trigger generation.

2.3.2.3 Hadronic calorimeter

The Hadronic Calorimeter (HCAL) [18] measures the energies and directions of particle jets, and provides hermetic coverage for measuring the missing transverse energy. Therefore the Hadron Barrel (HB) and the hadron end cap of the HCAL, which are located inside the solenoid, cover a pseudorapidity range of $|\eta|$ <3.0. The HB extends radially between $r = 1.80$ m and $r = 2.95$ m. In order to minimize multiple scattering for traversing muons, "low Z" materials are chosen. The active elements of the barrel and end cap hadronic calorimeter consist of plastic scintillator tiles with wavelength shifting fiber readout. Layers of these tiles alternate with layers of brass absorber to form the sampling calorimeter structures. Brass has been chosen, because it is non magnetic and has a reasonable interaction length of approximately 15 cm. The tiles are arranged in projective towers with fine granularity to provide good dijet separation and mass resolution. Since the thickness of the HB is only 6.5 interaction length, additional scintillators (hadron outer detector) are installed inside the muon barrel system. Since this part of the HCAL is outside of the solenoid it uses the coil as additional absorber. To extend the hermeticity of the HCAL up to $|\eta| = 5$, the hadron forward calorimeters are located 11.2 m from the interaction point.

2.3.2.4 Electro-magnetic calorimeter

The ECAL [19] determines the energy of electrons and photons and together with the HCAL it measures jets with high precision. A good energy resolution is crucial. To achieve the necessary angular separation, a highly granular design of the ECAL is required. Apart from high resolution and fast response for using the ECAL signal for trigger generation, the ECAL and its readout electronics need to be radiation tolerant. The chosen system consists of 75848 lead tungstate crystals ($PbWO_4$). This material was selected because it has a high density (8.2 g/cm^3) leading to a short radiation length[7] of $X_0 = 0.89$ cm and a small Moliere

[6] The hadronic equivalent of the electromagnetic radiation length (page 14) is the nuclear interaction length λ_0. It is much larger than the radiation length, e.g. in lead materials $\lambda_0/X_0 = 30$.

[7] The radiation length X_0 is determined as the longitudinal distance over which a relativistic electron or photon loses a fraction $(1 - \frac{1}{e}) \simeq 63\,\%$ of its energy through bremsstrahlung [15]. To calculate X_0 a fit to the

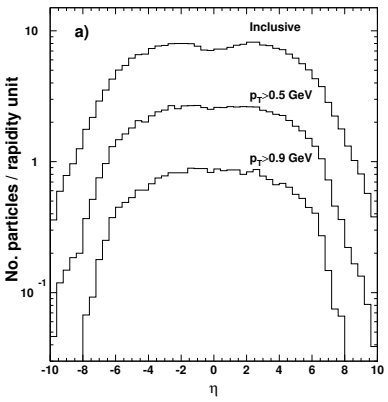

Figure 2.11: Pseudorapidity distribution of charged particles in minimum bias events [5].

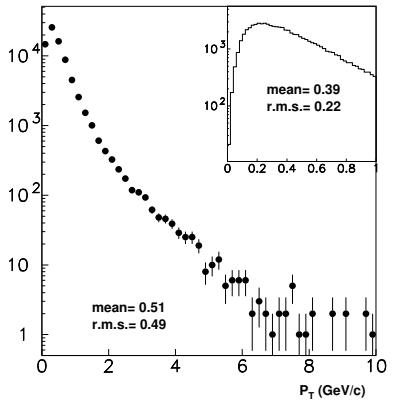

Figure 2.12: Transverse momentum of charged particles in minimum bias events [5].

radius[8] of $R_M = 2.19$ cm. This allows a compact ECAL design with narrow showers. $PbWO_4$ crystals emit 80 % of the light within 25 ns and the material is radiation hard up to 100 kGy (Sect. 2.4.6). Because of the low light yield of $PbWO_4$ and the strength of the magnetic field, the use of photomultipliers was not possible. The crystals of the barrel region are read out by silicon Avalanche Photodiodes (APDs) yielding avalanche gain. For the end cap region more radiation-hard vacuum phototriodes are used. The consequence of eq. 2.5 for the ECAL is, that for a given magnetic field $B = 4$ T and a given inner radius of $r = 1.29$ m a minimal transverse momentum p_{Tmin} exists, which must be exceeded by a particle to reach the ECAL. Particles with a lower momentum than $p_{Tmin} = 1.5$ GeV, so called "loopers", will describe a spiral trajectory parallel to the beam axis without causing occupancy in the ECAL. The distribution of the transverse momentum of charged particles from simulated minimum bias events is shown in Figure 2.12 [5]. The mean p_T is about 0.5 GeV, i.e. most of the particles will not reach the ECAL. In Figure 2.11 the number of tracks per η unit is plotted from minimum bias events. The plot is normalized to the number of particles per η unit and per pp event.

2.4 Central Tracker of the CMS Experiment

An important part of the CMS physics program relies on the capability of the detector to reconstruct charged particle tracks, and to measure with high resolution their momenta and their vertex of origin. Tracking within a strong magnetic field is a very powerful tool for the identification and accurate reconstruction of muons, electrons, and jets. Moreover, accurate vertex reconstruction is expected to play an important role in jet flavor tagging, especially

data can be used [3]:

$$X_0 = \frac{716.4 \text{ g cm}^{-2} A}{Z(Z+1)\ln(278/\sqrt{Z})} \tag{2.9}$$

Z is the atomic number and A is the atomic mass.

[8]The Moliere radius describes the lateral development of the electromagnetic shower in the crystal; 90 % (99 %) of the energy is contained within a cone with radius R_M ($3.5 \times R_M$) [15].

for b- and τ-jets. Therefore choice of detector technology must be adapted to the particle densities that will be present under the LHC running conditions: in the high luminosity regime, about 20 minimal bias events per bunch crossing (page 4) are expected to produce more than 1000 charged particles in the acceptance of the tracker ($|\eta|$ <2.5) [5]. Pattern recognition therefore demands highly granular detectors to keep the occupancy low and to achieve a high spatial resolution. In regions with a lower particle density, the strip length could be longer and the strip pitch could be wider. The charged track density under the impact of the 4 T magnetic field can be seen in Figure 2.10. The high track density in the range of small radii increased by "loopers" has important implications for the architecture of the CMS tracker [5] concerning the cell occupancy and the radiation tolerance of the used components.

2.4.1 Silicon Strip Detector

According to equation 2.8 the error in the transverse momentum measurement is proportional to $\sim 1/BL^2$. This means the CMS silicon strip detector with its 10 barrel layers and a large radial extension is the most important subdetector for the p_T determination. The silicon strip detector is shown in Figure 2.13. The barrel region consists of four inner layers (Tracker Inner Barrel, TIB) and six outer barrel layers (Tracker Outer Barrel). On each side of the TIB there are three mini disks (Tracker Inner Disk) and each end cap region consists of nine disks (Tracker End Cap). The strip detector covers the area from 20 to 120 cm in radius and from 0 to 280 cm in z-direction, corresponding to a pseudorapidity region of $|\eta|$ <2.5. Beyond this η value the charged track density will become too high to allow a good performance of the strip detector. The strip sensors are organized in modules of different shape and dimensions to match the requirements of the different parts in the device. The modules consist of the microstrip sensor, the readout electronics and the support structure. The pitches and strip length of the various sensors in the detector are determined by the resolution requirements (25 µm in the inner part, 50 µm in the outer part) and by the need to keep the cell occupancy below the level of 1 %. The TIB contains 320 µm thick sensors with a pitch in the range from 80 µm to 120 µm and length of the strips between 7 and 12.5 cm depending on the position of the module. The orientation of the strips is parallel to the beam axis and provides therefore the r-ϕ measurement. For the z-coordinate determination, the first two layers are double-sided equipped with back-to-back stereo detectors whose strips are tilted by 100 mrad. Due to the lower track density in the region of the TOB, the pitch is increased and varies from 120 to 180 µm and the length raises up to 21 cm. In order to maintain a good signal over noise (S/N) ratio, thicker silicon sensors are used in regions with larger strip areas. The TOB consists of 500 µm thick sensors and the first two layers are double-sided processed like the TIB sensors. The TEC is composed of nine large disks subdivided into seven rings each. The three outermost rings are equipped with 500 µm thick sensors and the four innermost ones with thin 320 µm sensors. The strips are arranged radially, pointing towards the beamline and therefore having a variable pitch. They are providing the ϕ measurement. For the r coordinate measurement the first, second and fifth ring are also equipped with stereo sensors. The TID is made out of three small disks that close the TIB. Sensors of 320 µm thickness like those in the inner part of the TEC are used.

The entire silicon strip detector consists of almost 15400 modules, which will be mounted

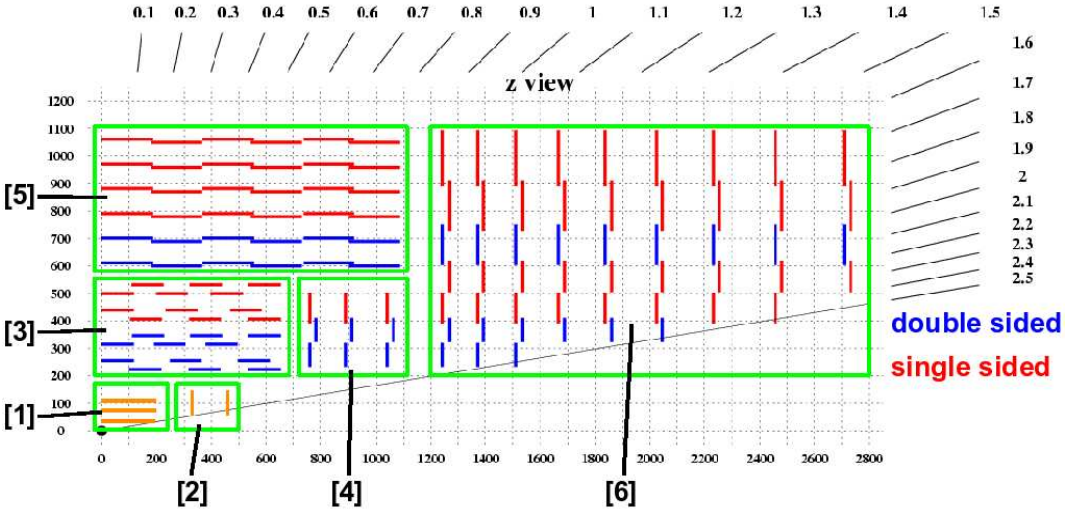

Figure 2.13: Longitudinal cross section of a quarter of the CMS central tracker. The different subdetectors are: [1] Pixel Barrel, [2] Pixel End Caps, [3] Tracker Inner Barrel (TIB), [4] Tracker Inner Disk (TID), [5] Tracker Outer Barrel (TOB), [6] Tracker End Caps (TEC).

on carbon-fiber structures. The operation temperature will be around -20 ℃ and for this reason the silicon strip detector is housed inside a temperature controlled outer support tube. The entire area, which is covered by the strip detector is about 170 m^2 (225 m^2 if the contribution of the stereo detectors is included) instrumented with about 10^7 channels. The channels are read out by charge sensitive amplifiers, whose output voltage is sampled at the beam crossing rate (40 MHz). The data are stored in a pipeline and after a trigger confirmation the data are transfered to the control room.

2.4.2 Pixel Vertex Detector

The most interesting events at the LHC are likely to contain several b-jets originating from the decay of heavy particles (Fig. 2.5). To allow an efficient tagging of these jets as well as of other objects (c, τ) the tracking must extend as closely as possible towards the interaction vertex. Because of the high track densities at these small distances pattern recognition arguments require the innermost tracking layers to be composed of pixel devices delivering true space point information with high resolution (Fig. 2.14). Over the full acceptance of the CMS detector the pixel system should provide two or more hits per track, which allow secondary vertices to be found for tagging long-lived objects, like b or c quarks and τ-leptons and to distinguish them against a large background of light quark- and gluon-jets. For detecting Higgs or SUSY particles b-tagging will play an important role as well as for conventional B-hadron physics including CP violation, B_s-oscillations, rare B-decays and top quark physics. The pixel detector will confirm or reject track segments measured by the outer tracker layers. Once a track has been successfully followed to the pixel layers, the three pixel hits will be crucial to extrapolate the tracks to the interaction vertex with high precision. Moreover the additional pixel hits can be used to improve the error of the p_T measurement performed by

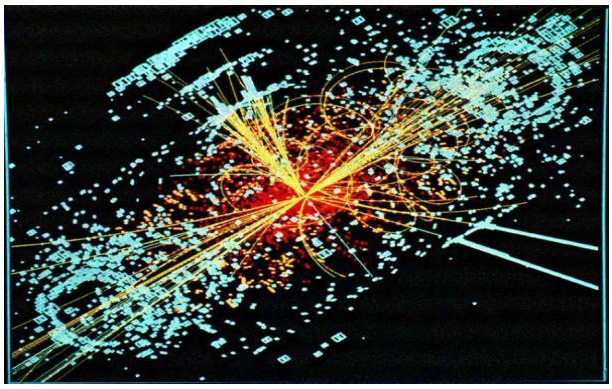

Figure 2.14: Simulation of a Higgs decay to two hadronic jets (upper center, 11 o'clock) and two electrons (lower right, 4 o'clock) in the CMS detector. The lines denote particles produced from the collision of a pair of ultra-high energy protons. Energy deposits of the particles in the detector are shown in pale blue.

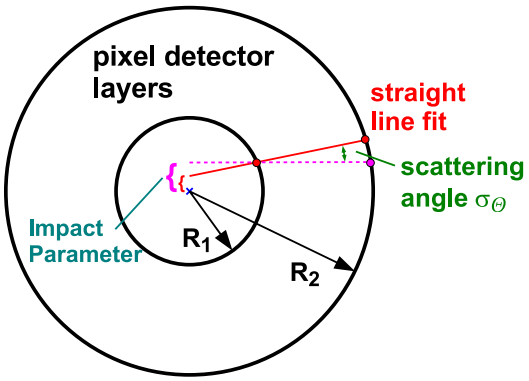

Figure 2.15: Impact parameter determination with a straight-line fit using two barrel layers of the pixel detector.

the silicon strip detector. By a precise reconstruction of the secondary vertex from the decay of short flight-path particles, the lifetime of these particles can be determined.

To get a quantitative feeling for the requirements on the vertex detector, the track Impact Parameter (IP) resolution, relevant to b-jet identification and lifetime measurements, is discussed in detail. The impact parameter is the shortest distance of a reconstructed particle trajectory from the vertex in the transverse plane. For simplification just two barrel layers are assumed (Fig. 2.15) and the error of the impact parameter (σ_{IP}) can be estimated by the error of a straight-line fit:

$$\sigma_{IP}^2 = \left(\frac{n}{n-1}\right)^2 \sigma_{layer1}^2 + \left(\frac{1}{n-1}\right)^2 \sigma_{layer2}^2 \qquad \text{with:} \qquad n = \frac{R_2}{R_1} \tag{2.10}$$

According to this equation, the error of the IP depends not on the absolute radii of the layers but on the ratio $n = R_2/R_1$. In the case of a large n, the second summand becomes

negligibly small and the dominating contribution to the error is the spatial resolution of the pixel detector layer 1. Due to the factor $n/(n-1)$, the error of the IP is in the best case as big as the error of the pixel detector. A large ratio of R_2/R_1 is achieved with a small R_1 and a large R_2. If one takes multiple scattering[9] at the inner layer into account, then equation 2.10 becomes:

$$\sigma_{IP}^2 = \left(\frac{n}{n-1}\right)^2 \sigma_{layer1}^2 + \left(\frac{1}{n-1}\right)^2 \sigma_{layer2}^2 + R_1^2 \sigma_\Theta^2 \tag{2.12}$$

where R_1 is the radius of the scattering layer and σ_Θ is the standard deviation of the scattering angle Θ. By means of this extra term the crucial impact of the material budget on the error of the IP determination is obvious. After these considerations of the error of the impact parameter determination, three design parameters of the pixel vertex detector are crucial:

- The ratio of the distances ($n = R_2/R_1$) of the layers from the interaction region should be as great as possible under the additional requirement that the innermost layer is as close as possible to the interaction point and the radius of the second layer is as large as possible.
- The intrinsic hit resolution of the pixel vertex detector.
- The material budget to minimize the probability of multiple scattering.

When optimizing these parameters design constraints have to be taken into account:

- The pixel size is influenced by the area needed on the readout chip for the pixel analog front-end and readout circuitry.
- The extremely high power density, requiring efficient cooling, and the necessary mechanical stability of the sensor frames will determine the material budget.
- The radiation environment close to the interaction region limits the lifetime of sensor and readout chip.

The minimal radius is defined by the beam pipe radius plus a clearance needed for inserting and removing the pixel detector for yearly beam pipe back-outs. The outer radius of the beam pipe is 30 mm. A consequence of the small R_1 is the increasing charged track density, which is proportional to $1/r^2$ (Fig. 2.10) and causes a higher pixel occupancy combined with a higher radiation dose. R_2 should be as large as possible, but the cost of a layer increases with its area which is proportional to the radius in the case of a cylinder. Hence the maximal radius is a compromise between financial matters and gain in the reduction of the error in the IP determination. The spatial resolution of the pixel detector is related to the geometrical pixel

[9] For a thin layer of traversed material the standard deviation of the projected scattering angle of a particle with charge z can be approximated by:

$$\sigma_\Theta = \frac{13.6 \text{ MeV}}{p\beta c} z \sqrt{\frac{x}{X_0}} \left(1 + 0.038 \ln \frac{x}{X_0}\right) \tag{2.11}$$

x/X_0 is the thickness of the scattering medium in X_0 (page 14), p is the momentum and β is the velocity of the particle [3].

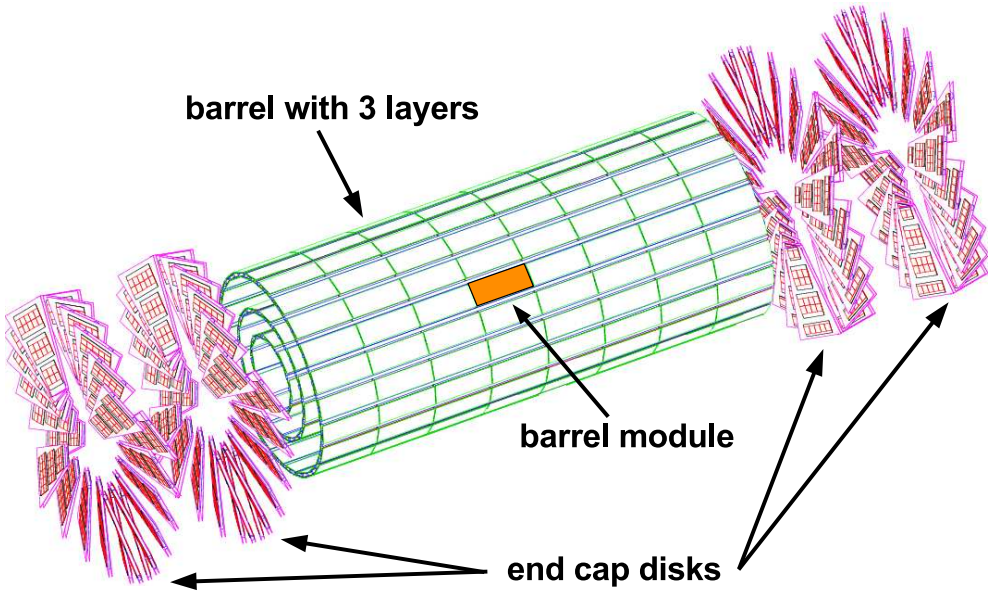

Figure 2.16: The CMS pixel vertex detector consists of three barrel layers and two sets of two end cap disks.

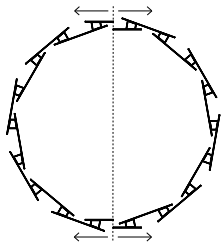

Figure 2.17: Radial cut of the innermost layer.

size and can be improved by analog signal readout to profit from position interpolation, where the effect of charge sharing among pixels is present. In the barrel region the charge sharing in r-ϕ-direction is improved due to the very high magnetic field in CMS. The electrical field in the sensor and the magnetic field of CMS are perpendicular and cause a Lorentz force on drifting e^- in r-ϕ-direction (Sect. 3.2.3.2).

The chosen design for the pixel vertex detector represents a compromise of all requirements and constraints mentioned above. Finally the pixel vertex detector consists of three barrel layers with two end cap disks on each side of them (Fig. 2.16).

The pixel system will be inserted along the z-axis after the beam pipe baked out prior. The diameter of the beam pipe is increasing with $|z|$. Therefore the layers consist of two half cylinders which allows the insertion and removal of the pixel system separable into a left and a right half with respect to the beam axis. The mean radii of the barrel layers are 44.4 mm, 73.3 mm and 102 mm and the length of the sensitive part of the barrel is 53.3 cm. The layers are planked with 128, 224 respectively 320 full modules in addition to 32 half modules per layer. In total the pixel detector barrel will consist of 672 full modules and 96 half modules. The half modules are necessary, because the layers consist of two half cylinders with half modules at the azimuthal edges (Fig. 2.17). The detailed numbers of the barrel layers can be seen in Table 2.2. The cylindrical shape of the barrel is guaranteed by trapezoidal cooling tubes held in place by two end-flanges [5]. The modules are mounted on carbon fiber blades which are alternating glued to two thin-walled aluminum cooling tubes from inside and outside. This facet like design causes an overlap of the faces in r-ϕ-direction. The faces consist of the carbon fiber blades with the modules. On each face 8 modules are fixed by small screws, using thermally conductive paste to improve heat conductance. In addition to the 84 faces with full modules for the entire pixel barrel there are 12 half carbon

Radius (mm)	No. faces	No. Modules	No. Readout Chips	No. Pixels ($\times 10^6$)	Area (m^2)
41-46	16 + 4 ($\frac{1}{2}$)	128 + 32 ($\frac{1}{2}$)	2304	9.6	0.15
70-76	28 + 4 ($\frac{1}{2}$)	224 + 32 ($\frac{1}{2}$)	3840	16	0.25
99-104	40 + 4 ($\frac{1}{2}$)	320 + 32 ($\frac{1}{2}$)	5376	22.4	0.35
total	84 + 12 ($\frac{1}{2}$)	672 + 96 ($\frac{1}{2}$)	11520	48	0.75

Table 2.2: Parameters of the CMS pixel detector barrel. The numbers of the faces and the modules are split in full and half faces respectively modules.

fiber blades (half faces) each assembled with 8 half modules. The detailed build up of the modules and the electrical performance of them is subject of the following paragraphs. The two end disks, extending from 6 to 15 cm in radius, are placed on each side of the barrel at $|z| = 34.5$ cm and 46.5 cm. Each of the four disks include 24 wedge-shaped blades, which are arranged in a turbine-like geometry. Therefore geometric and $E \times B$ charge sharing effects are induced by rotating the blades by 20° around their radial symmetry axes (Sect. 3.2.3.2). This is necessary since in the forward region the electrical field and the magnetic field are parallel and most particles close to normal incidence. Each blade has 7 different plaquettes (Table 2.3) and in total the end cap disks comprise 672 plaquettes. Each blade consists of two

z (cm)	Radius (mm)	No. Blades per disk	No. Plaquettes per blade	No. Readout Chips per disk	No. Pixels per disk ($\times 10^6$)	Area per disk (m^2)
± 34.5	60-150	24	7	1080	4.5	0.071
± 46.5	60-150	24	7	1080	4.5	0.071

Table 2.3: Parameters of the CMS pixel detector end disks.

low-mass trapezoidal structures made with two carbon-fiber panels. Between the two panels runs a U-shaped cooling tube. On the panels up to seven plaquettes are glued, which consist of a sensor with readout chips and a low mass flexible printed circuit board.

In the design specifications for the silicon vertex detector [5] it is postulated that the detector material has to survive the fluences up to 6×10^{14} n_{eq}/cm^2 without any unacceptable degradation in performance[10]. This means for the innermost layer of the barrel, that it has to be replaced after the first four years of LHC operation (assuming that the first three years of LHC operation will represent roughly one year of high luminosity, and high luminosity operation starts in year 4). Practically the fluence of 6×10^{14} n_{eq}/cm^2 is just a soft limit and the decision to replace the modules will be based on the performance of the sensor and the readout chips. The expected radiation levels for the different layers of the tracker barrel are listed in Table 2.4.

[10]The fluence of 6×10^{14} n_{eq}/cm^2 seemed to be reasonable at that time, since the radiation-hard DMILL [20] process, used for designing prototype structures, was certified up to 100 kGy which corresponds to about 6×10^{14} n_{eq}/cm^2. For the conversion of radiation dose to fluence see Section 3.2.1. All particle fluences are normalized for comparison and scalability to 1 MeV neutrons (n_{eq}/cm^2).

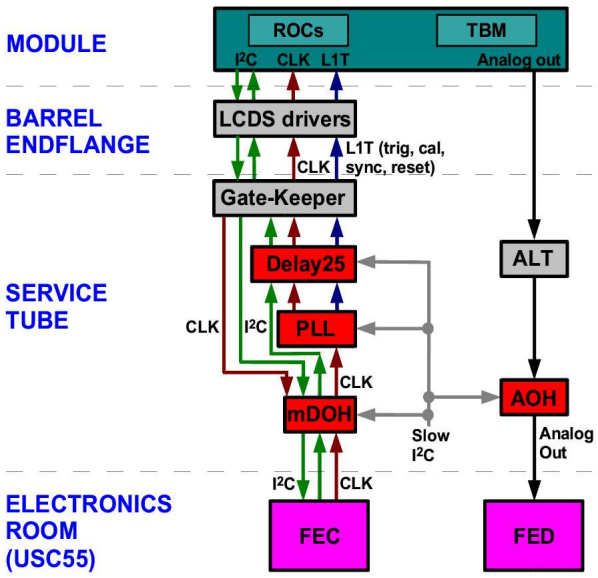

Figure 2.18: Readout and control scheme of the pixel vertex detector.

2.4.3 Readout and Control System

The pixel detector readout and control scheme is shown in Figure 2.18 [21]. The readout chain transfers the data from the front-end electronics to the Front-End Driver (FED). The control chain transmits the control signals from the Front-End Controller (FEC) to the front-ends. The FED and FEC are located in the electronics room 100 m away from the detector. The connection between the front-ends and the FED/FEC is provided by optical links [22], analog for the readout part and digital for the control part. The most important front-end components are the Readout Chip (ROC) and the Token Bit Manager control chip (TBM). Both are placed on the detector modules and described in more detail in Chapter 3.

The readout system transfers the data from the front-end to the electronics room. The analog data from the modules are brought by the signal cable and the barrel end flange print to the Analog Level Translator chip (ALT). The ALT amplifies the signals. The Analog Optical Hybrid (AOH) converts the signal in an analog optical signal and transmits it via an optical link. Both the ALT and the AOH are mounted on the pixel service tube. The optical signals are received by the FED. The FED [23] is a readout unit that will digitize the analog input signals, build event fragments and send them to the CMS data acquisition system. The number of readout optical links has to be optimized. On one hand the number has to be kept as small as possible in order to minimize the amount of material and the cost. On the other hand the data transfer capacity has to be sufficient to avoid large data losses. On the innermost two layers 8 ROCs and on the outermost layer 16 ROCs will be read out by an optical link. A total number of 1120 optical links are planned to read out the barrel pixel detector. For the entire pixel detector including the forward disks, 40 FEDs are needed. Since maximum 36 links can be attached to a single FED. The FEDs are set up in three VME crates in the electronics room.

The control system sends the 40 MHz clock, the trigger and the control signals (e.g. reset)

to the front-end electronics. Moreover the control system has to program all front-end devices i.e. all ROCs and TBMs. The FEC [24] is connected by optical fiber Control Networks (CNs) to the front-ends. On the front-end side the optical signals are converted to electrical signals by the Digital Optical Hybrid (DOH). There are several other Application Specific Integrated Circuits (ASICs) between the DOH and the module (Fig. 2.3). The Phase Locked Loop chips (PLLs) [25] are used to separate the clock from the trigger. The trigger information is encoded as a missing clock signal. The DELAY25 [26] chips adjust the relative phases of all control signals. The Gate-Keeper chips convert the LVDS (Low Voltage Differential Signaling) signals to LCDS (Low Current Differential Signaling) used by the pixel front-end chips. Finally the LCDS-Driver chips are used to drive the signals to each module. In addition these chips are used to compensate the signal phases for the different signal cable length. The pixel detector will have in total 64 CNs and most of them are controlling 12 modules. Each FEC can service up to 16 CNs and all FECs are set up in a VME crate. The VME FEC crates will get the data from the TTC system [27]. The programming of all ROCs and TBMs requires to download a large data volume. To fulfill this task the industrial I^2C protocol [28] was modified. The main modifications include the increase of the clock speed to 40 MHz and dropping the requirement of an acknowledge signal. Besides the pixel specific devices a number of standard CMS components like PLLs, AOHs and others have to be controlled. This is done with the standard CMS CCU token-ring [29] system, indicated by "slow I^2C" in Figure 2.18.

2.4.4 Performance

The Central Tracker as described in Section 2.4.1 and Section 2.4.2, provides the following resolutions:

- The single-point resolution of the Tracker Inner Barrel (TIB) is between 23-34 µm in the r-ϕ-direction and 23 µm in the z-direction [30]. With the single-point resolution the error of the transverse momentum can be calculated (eq. 2.8).

- The single-point resolution of the Tracker Outer Barrel (TOB) is between 35-52 µm in the r-ϕ-direction and 52 µm in the z-direction [30].

- The spatial resolution of the pixel vertex detector is measured to be about 10 to 20 µm for the r-ϕ-direction (direction of the Lorentz drift) depending on the radiation dose (Sect. 3.2.3.4). After irradiation with 6×10^{14} hadrons per cm^2, corresponding to one year high luminosity operation, the resolution is still better than 20 µm. The spatial resolution in the direction transverse to the Lorentz drift varies in the range of 20 to 40 µm and weakly depends on the irradiation dose [31]. The Lorentz angle is about 23° and improves the r-ϕ resolution through charge sharing [32].

- The material budget of the final design of the pixel vertex detector barrel was calculated to be about $x/X_0 = 1.6$ % per layer averaged over ϕ at about $\eta = 0$ [33] (Fig. 2.22 and Sect. 3.3). This calculation is based on a detailed description of the geometry of the barrel module and the mechanical support structure including the coolant. For a detailed description, see Section 2.4.5.1.

In Section 2.4.2 the error of the impact parameter was derived for a simplified pixel vertex detector containing two barrel layers. The error was estimated by the error of a straight-line fit (eq. 2.10). With the radii of the final design and the recently mentioned spatial resolutions it can be calculated (Sect. 2.2):

$$\sigma_{IP}^2 = \left(\frac{n}{n-1}\right)^2 \sigma_{layer\,1}^2 + \left(\frac{1}{n-1}\right)^2 \sigma_{layer2}^2 \quad \text{with:} \quad n = \frac{R_2}{R_1} = \frac{10.2 \text{ cm}}{4.4 \text{ cm}} = 2.32$$

$$\Rightarrow \sigma_{IP} = 38.3 \text{ µm} \quad \text{for} \quad \sigma_{layer1/2} = 20 \text{ µm} \tag{2.13}$$

$$\Rightarrow \sigma_{IP} = 19.2 \text{ µm} \quad \text{for} \quad \sigma_{layer1/2} = 10 \text{ µm} \tag{2.14}$$

Taking into account the probability for multiple scattering at the inner layer of the pixel detector, one can calculate the error of the projected scattering angle with equation 2.11. Therefore one has to use the scattering length of a pixel detector layer (1.6 %) and assume a particle e.g. a muon with a momentum[11] of 2 GeV/c. Doing this, one gets:

$$\sigma_\Theta = \frac{13.6 \text{ MeV}}{p\beta c} z \sqrt{\frac{x}{X_0}} \left(1 + 0.038 \ln \frac{x}{X_0}\right) \quad \text{with:} \quad p = 2 \text{ GeV/c} \quad \text{and:} \quad z = 1$$

$$\Rightarrow \sigma_\Theta = 847 \text{ µrad} \tag{2.15}$$

Using the equation 2.12 for the determination of the error of the IP with the effect of multiple scattering, the error becomes:

$$\sigma_{IP} = 53.4 \text{ µm} \quad \text{for} \quad \sigma_{layer1/2} = 20 \text{ µm} \tag{2.16}$$

$$\sigma_{IP} = 41.9 \text{ µm} \quad \text{for} \quad \sigma_{layer1/2} = 10 \text{ µm} \tag{2.17}$$

Comparing the results for the error with and without multiple scattering, one realizes, that for a transverse momentum of 2 GeV, the multiple scattering contribution to the error is dominating. By neglecting the contributions from the terms concerning the spatial resolution of the pixel detector and taking just into account the multiple scattering part, one gets with equation 2.12 already an error of 37 µm for the IP compared with 53.4 µm respectively 41.9 µm. This fact justifies the effort to minimize the amount of material of the pixel vertex detector. The CMS track reconstruction method described in Reference [34], achieves for a muon with a transverse momentum of 1 GeV/c at $\eta = 0$ a transverse IP resolution of about 90 µm. The straight-line fit gives for this momentum $\sigma_{IP} = 84$ µm for $\sigma_{layer1/2} = 20$ µm and $\sigma_{IP} = 77$ µm for $\sigma_{layer1/2} = 10$ µm. Estimating the contribution of the 1 mm thick beryllium beam pipe at a radius of 30 mm to the multiple scattering one gets an approximately 10 % higher error in the IP resolution. Hence the beam pipe could explain the better result of the

[11] A muon with a transverse momentum of 2 GeV/c is a conservative assumption and hence the $\sigma_\Theta = 847$ µrad presents the worst case. For a muon with $p_T = 10$ GeV/c the $\sigma_\Theta = 145$ µrad. Without any other contributions σ_{IP} is for this case 6.4 µm and thus no longer dominating. On the other hand the assumption of $x/X_0 = 1.6$ % is only for $\eta \approx 0$ realistic (Fig. 2.20).

simple example. For higher transverse momenta of 10 GeV/c (100 GeV/c) the IP resolution of the track reconstruction software is about 20 µm (10 µm) compared to 39 µm (38.3 µm) from the simple straight-line fit. The contribution of the multiple scattering term in equation 2.12 decreases with $1/p_T$ (eq. 2.11). Therefore the best IP resolution one could get with the straight-line fit is 38.3 µm for $\sigma_{layer1/2} = 20$ µm (eq. 2.14).

In order to judge if these spatial resolutions are satisfactory to fulfill the goals of the physics program of LHC, a closer look on an example is taken. The b-physics program is chosen (Sect. 2.2) because it will begin immediately after LHC startup since already at low integrated luminosity a reasonable amount of events is expected. To investigate CP violation, B_s-oscillations and rare B-decays, tagging and reconstructing in detail b-jets is essential. This requires the ability to identify unambiguously tracks coming from multiple vertices, the ability to reconstruct a variety of decay chains and the accurate determination of the b decay proper time, based on the characterization of displaced vertices and the kinematics of the associated tracks. More information can be found in [35], where the investigation of the channel $B_s^0 \rightarrow (J/\Psi)\Phi \rightarrow \mu^+\mu^- K^+ K^-$ with the CMS detector is studied in detail. The present average values of the mean lifetime and the mass of the B_S^0 meson is $\tau_S = 1.466 \pm 0.059$ ps respectively 5369.6 MeV [36]. The mean energy of the B_s^0 mesons produced at the LHC can be estimated as approximately 24.5 GeV [35]. The mean flight path of the B_s^0 meson in the frame of the CMS detector can be therefore estimated as 1.99 mm. The observation of the mean lifetime with an accuracy of 10 % requires a resolution of about 44 µm on the proper decay length in the rest frame of the B_s^0 meson and a resolution of about 200 µm of the mean flight path in the frame of the CMS detector. In addition, the decay of $B_s^0 \rightarrow (J/\Psi)\Phi \rightarrow \mu^+\mu^- K^+ K^-$ allows to study particle-antiparticle oscillation in the B_s^0-$\bar{B}_S^0$ system. The B_s^0 mesons are produced in strong interaction in one of the flavor eigenstates B_s^0 or $\bar{B}_s^0$, which are not the CP eigenstates. In the absence of CP violation, the mass eigenstates are also the CP eigenstates which are denoted B_{SH}^0 for the *heavy* and B_{SL}^0 for the *light* state. Due to the difference in the mass eigenstates, there is a time-dependent probability amplitude to observe an initially produced B_s^0 meson as B_s^0 or $\bar{B}_S^0$ at the time t. The present experimental lower limit on the difference of masses of heavy and light mass eigenstates of the B_s^0 meson is $\Delta m^{12} > 14.4$ ps^{-1} at 95 % C.L. [37]. For a mass difference of 14.4 ps^{-1}, the period of oscillation can be estimated as T = 0.43 ps, which corresponds to the flight path of $L^{pr-sec} = 130$ µm in the rest frame of the B_s^0 meson or approximately $L^{lab} = 591$ µm in the detector frame. In this case the resolutions of 13 µm on the proper decay length and of 59 µm on the flight path in the detector frame is required to observe the B_s^0-$\bar{B}_S^0$ oscillations directly with a precision of 10 %. However recent experimental results suggest the value for the mass difference to be even larger [38]. Obviously, for higher mass differences and hence faster oscillations, a higher accuracy is required. The newest publication from CDF claim a mass difference of 19.9 ps^{-1} [39]. This corresponds to a oscillation period of 0.32 ps and requires for a 10 % accuracy measurement a spatial resolution of 43 µm in the detector frame. The calculated errors of the impact parameter were $\sigma_{IP} = 53.4$ µm and $\sigma_{IP} = 41.9$ µm for an initial spatial resolution of the pixel vertex detector of $\sigma_{layer1/2} = 20$ µm respectively $\sigma_{layer1/2} = 10$ µm. Even in the case of this simple example, assuming only two pixel layers and performing a straight-line fit, it seems to be

[12] $\Delta m_{B_s^0} = m_{B^0_{SHeavy}} - m_{B^0_{SLight}}$; $\Delta m_{B_s^0}$ is a measure of 2π times the B_s^0-$\bar{B}_S^0$ oscillation frequency in time-dependent mixing experiments. Unit of $\Delta m_{B_s^0}$: $10^{12}\hbar\text{s}^{-1} = \hbar\text{ps}^{-1}$ [37].

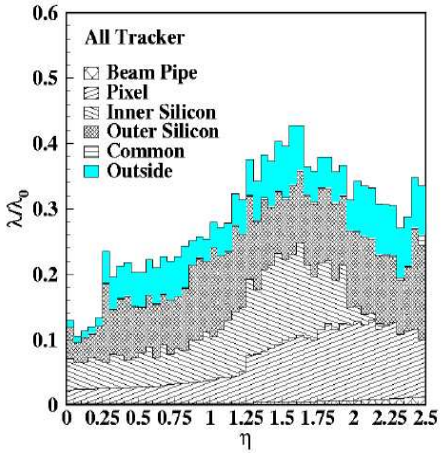

Figure 2.19: Material budget of the CMS tracker in terms of interaction length as function of η for the different tracker subunits.

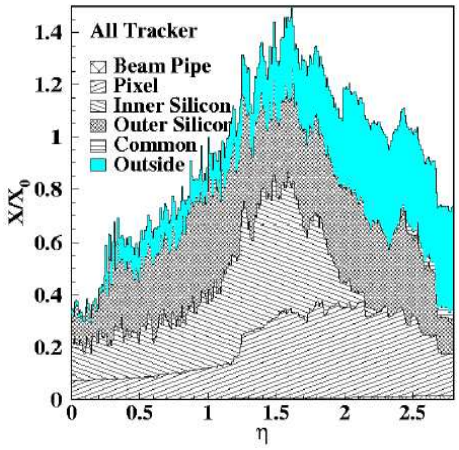

Figure 2.20: Material budget of the CMS tracker in terms of radiation length as function of η for the different tracker subunits.

reasonable to achieve the required accuracy for measuring the oscillation frequency of the B_s^0-$\bar{B}_S^0$ system and determine the mean lifetime of the B_s^0 meson by distinguishing between the primary interaction point and the secondary vertices. Taking into account, that the spatial resolution gets worse with the accumulated radiation dose in the pixel detector sensors [32] and that the discovery potential for various Higgs channels require a high integrated luminosity (Fig. 2.4), it is an advantage of the b-physics program to work at low luminosity operation during the first years of LHC. But the ability to distinguish b-jets originating from primary or secondary vertices is also crucial for Higgs search to suppress background processes which include b-jets too.

2.4.5 Material Budget

Apart from the sensitive detector volumes, the CMS tracker contains a lot of non-sensitive material, like mechanical supports, electrical supply cables and cooling services. For $1.2< |\eta| <2.1$ this material can constitute of more than one radiation length, as can be seen from Figure 2.20. In addition the nuclear interaction length is shown in Figure 2.19. The amount of material in the tracker must be kept as low as possible in order to avoid secondary interactions, excessive multiple scattering, bremsstrahlung and photon conversion which would compromise the performance of the electromagnetic calorimeter. Therefore a compromise has to be sought between the number of hits per track (the number of active layers) for an efficient track reconstruction and the amount of material in the tracker. Also the cable-routing has to be carefully studied in order to minimize its impact on the tracker and ECAL performance. The gradually increase of the amount of material with respect to η is caused by the increasing path length of the tracks traversing the different layers of the tracker under a shallow angel and the mechanical support structures at $|z|$ of the different detector components (pixel barrel, TIB, TOB). At large η, not all layers are traversed by the tracks and thus the amount of material decreases again.

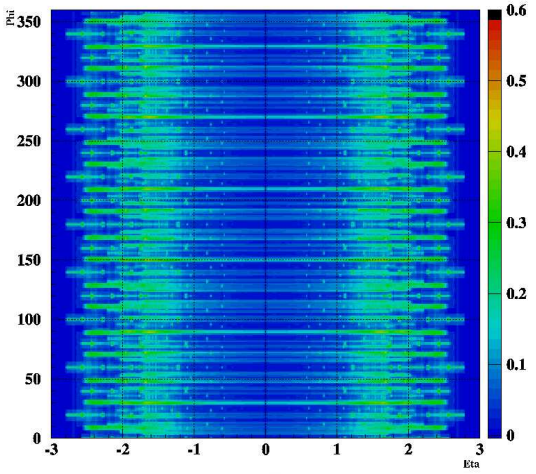

Figure 2.21: Material budget for three layers of the pixel vertex detector including the end-flange structures in units of X_0 (color coded). The MB is calculated as a function of the azimuthal angel ϕ versus the pseudorapidity η [33].

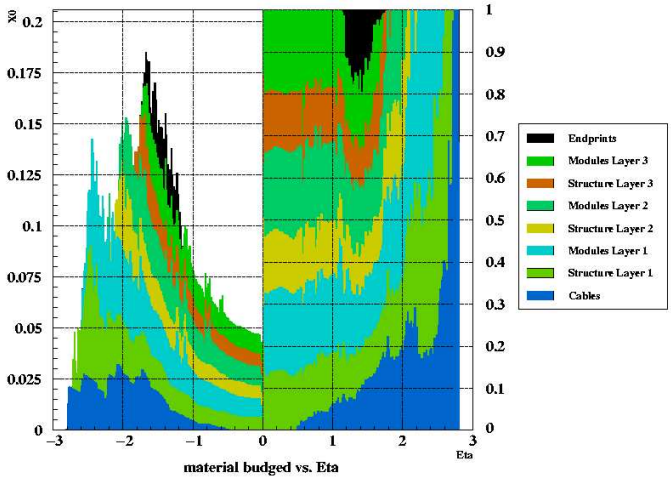

Figure 2.22: Left: Total material budget of the pixel vertex detector in units of X_0 as a function of the pseudorapidity. The MB is averaged over ϕ and subdivided in the contributions of the different layers [33]. Right: The different contributions to the MB as a function of η is shown.

2.4.5.1 Material budget of the pixel vertex detector

The Material Budget (MB) of the pixel vertex detector is a crucial parameter with respect to the error of the IP determination (Sect. 2.4.4). The distribution of the material for the final design of the pixel detector consisting of three layers in combination with the mechanical support structure of the barrel including the end-flange structures is shown in Figure 2.21. The MB in units of x/X_0 is plotted as a function of the azimuthal angel and the pseudorapidity. The calculation for the MB is based on a detailed geometrical description of the module and the support structure including the coolant (C_6F_{14}) and all the cabling [33]. The different materials of the design are taken into account with their specific radiation length and mass distribution. The increase of the amount of material in the range of $1.2 < \eta < 2.5$ for the entire ϕ range is due to the mechanical structure, the end-flange structures and the cabling of the pixel barrel. This effect is intensified by the end-flange printed circuit boards and all connectors and components assembled to it. Additionally the increasing path length for transversing the modules with cumulative η are visible. For some specific ϕ values the MB is higher due to the cooling tubes filled with coolant and partly superimposed with structures from other layers e.g. cable and tubes (horizontal stripes in Fig. 2.21). The dip at $\eta = 0$ (Fig. 2.22) can be explained by the fact, that there is no overlap of the modules in z-direction, which results in an gap of about 400 µm. The remaining x/X_0 at $\eta = 0$ is caused by the coolant, the cooling tubes and the carbon fiber blades. The smaller peaks up to $\eta = 1.5$ are caused by the relatively massive high voltage capacitors for filtering the bias voltage of the sensors. In Figure 2.21 these capacitors can be seen, distributed over ϕ, as quadratic shaped objects. A more detailed breakdown of the material budget of the module can be found in

Section 3.3.

2.4.6 Radiation Levels

As a result of the large number of 20 minimum bias events and the resulting 1000 charged particle tracks per bunch crossing, the high radiation level requires radiation-hard detectors and front-end electronics. In addition this effect was intensified by the compact design of CMS and the choice of the strong magnetic field, which increased especially the track density of the central tracker (Fig. 2.10). The expected radiation levels in CMS for the silicon tracker barrel are given in Table 2.4 for an integrated luminosity of 500 fb^{-1}. A particle fluence of 4×10^{14} n_{eq}/cm^2 is for the innermost layer of the pixel detector equal to about 100 kGy. For details of the conversion of the particle fluence to the radiation dose see Section 3.2.1.

Radius (cm)	Fluence of fast hadrons ($10^{14}cm^{-2}$)	Dose (kGy)	Charged Particle Flux ($cm^{-2}s^{-1}$)
4	32	840	10^8
10	4.6	190	
22	1.6	70	6×10^6
75	0.3	7	
115	0.2	1.8	3×10^5

Table 2.4: The expected hadron fluences and radiation doses in different layers of the CMS tracker barrel for an integrated luminosity of 500 fb^{-1} (about 10 years). All particle fluences are normalized to 1 MeV neutrons (n_{eq}/cm^2).

2.5 Trigger and Data Acquisition System of CMS

The LHC bunch crossing rate of 40 MHz leads to approximately 10^9 events/sec at design luminosity. Data from only about 100 events/sec can be written to the disks which means a data rate of about 100 MB/s. Since one event producing approximately 1 MB of raw data [40] the trigger system has to achieve a rejection factor of nearly 10^7. The CMS trigger system consists of two levels. First, the rate is reduced from 40 MHz to 100 kHz by the Level-1 Trigger (L1T) logic in 3.2 µs. The L1T exploits only a small subset of data with low resolution and coarse granularity information from the muon system and macro granular energy resolution from the calorimetry to construct "trigger candidates". For each of the trigger candidates, a position and transverse momentum measurement is provided and threshold cuts in transverse momentum p_T are applied in order to select the most interesting events. While the L1T decision is being taken, the detector data must be held in pipeline memories until these data are confirmed or rejected by the L1T. The L1T decision is taken after a fixed latency of 128 bunch crossings i.e. in 3.2 µs. If there is no L1T issued after passing the latency, the data are overwritten in all subdetectors. The second step of the triggering system is the High Level Trigger (HLT). It takes over the data confirmed by the L1T and processes the data more completely using commercial processors. The HLT cuts down the 100 kHz to 100 Hz

by performing a sophisticated but still partial reconstruction of the events with additional information from the tracker to perform an online analysis allowing the identification of the physics process. At that level again, data confirmed by the L1T but not by the HLT, are permanently discarded.

2.6 Summary

The Large Hadron Collider (LHC) is a circular 7 TeV proton - 7 TeV proton collider with a bunch crossing frequency of 40 MHz and a design luminosity of 10^{34} cm^{-2}s^{-1}. For heavy ion operation the center-of-mass energy will be 1148 TeV. The LHC will allow to explore new physics at the TeV scale. Its physics program includes investigations of the limits of the Standard Model (SM), searches for the SM and the Supersymmetric (SUSY) Higgs bosons, searches for SUSY partners of the SM particles and high precision B-physics as well as heavy ion physics. In various decay channels of the SM and SUSY Higgs bosons b- and τ-jets will be present.

At four interaction regions experiments are being constructed including the Compact Muon Solenoid (CMS) detector. CMS is a multi purpose detector, featuring a large solenoidal magnet producing a 4 T field, a high-performance muon system, a full silicon tracker, a crystal Electro-magnetic Calorimeter (ECAL) and a hermetic Hadronic Calorimeter (HCAL). The muon system allows the efficient triggering, the identification and the measurement of muons. The HCAL performs a good measurement of the missing transverse energy due to its high hermeticity. The ECAL provides an accurate measurement of electron and photon energies and their directions of flight. The CMS tracker contains the silicon strip detector and the silicon pixel detector. The silicon strip detector has a good position resolution and a low cell occupancy, allowing track reconstruction and transverse momentum (p_T) measurement with very high efficiency.

The average number of inelastic pp collisions per bunch crossing is about 20. Therefore about 1000 charged tracks per bunch crossing will emerge from the interaction point of CMS. For pattern recognition the pixel detector delivers true space point information. For the Impact Parameter (IP) determination and the vertex reconstruction (primary and secondary vertices) with high precision tagging of $\tau's$ and b-jets is performed by the silicon vertex detector. The error of the IP gets smaller when the innermost layer is as close as possible to the interaction point and the outer layer has a radius as large as affordable. Since the error of the IP increases with multiple scattering, the amount of material of the detector layers is a crucial issue. In addition the intrinsic spatial resolution of the pixel sensor affects the error of the IP. Because of the high track density close to the interaction point (40 MHz/cm^2 for high luminosity and the innermost layer), the pixel detector needs a high granularity to keep the occupancy low and to achieve a high spatial resolution. On the other hand the pixel detector must be radiation tolerant up to a fluence of 6×10^{14} n$_{\mathrm{eq}}$/cm^2 (~ 100 kGy) corresponding to the first four years of LHC operation.

The barrel of the pixel vertex detector consists of three layers with in total 672 full and 96 half modules. The mean radii of the layers are 44.4 mm, 73.3 mm and 102 mm. The total area covered by the sensors is 0.75 m^2 which is segmented in 48×10^6 readout channels.

Chapter 3

Module of the Pixel Vertex Detector

The fundamental concept of a semiconductor particle detector is, that free electrons and holes may be generated by the lifting of electrons from the valence band into the conduction band. This can be accomplished by various mechanisms that have to provide the necessary energy, such as thermal agitation, optical excitation and ionization by penetrating charged particles. Position sensitivity is obtained by segmenting the sensor in small subsensors that are read out separately. After inducing the charge, the readout electronics measure the signal and serve the information for further processing. Hence the main components of the hybrid silicon vertex detector are the sensor and the readout chip. For practical reasons, the pixel detector is fragmented into subdetectors. The basic building block of the barrel part of the pixel vertex detector is a module. The modules are the smallest elements of the final pixel detector which can be operated as stand alone "mini" detector with full functionality. Therefore the commissioning and investigation of a module is an important step on the way to the final pixel detector. In Figure 3.1 a complete barrel module is shown. The half modules have the same design and functionality, but consist instead of two rows with 16 readout chips just of a single row with 8 readout chips (Fig. 3.2). Caused by the barrel design (Sect. 2.4.2), there are two different types of half modules required. Since the half faces are glued from inside or outside on the cooling tubes (Fig. 2.17). For the rest of this thesis pixel detector refers to

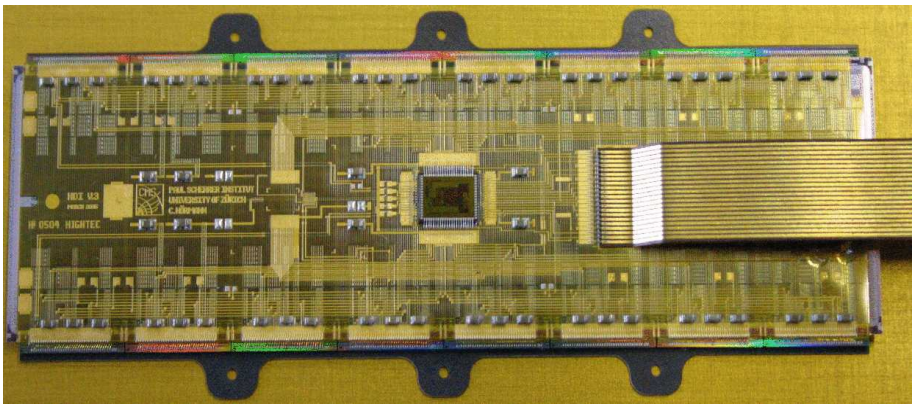

Figure 3.1: Final barrel module for the pixel vertex detector.

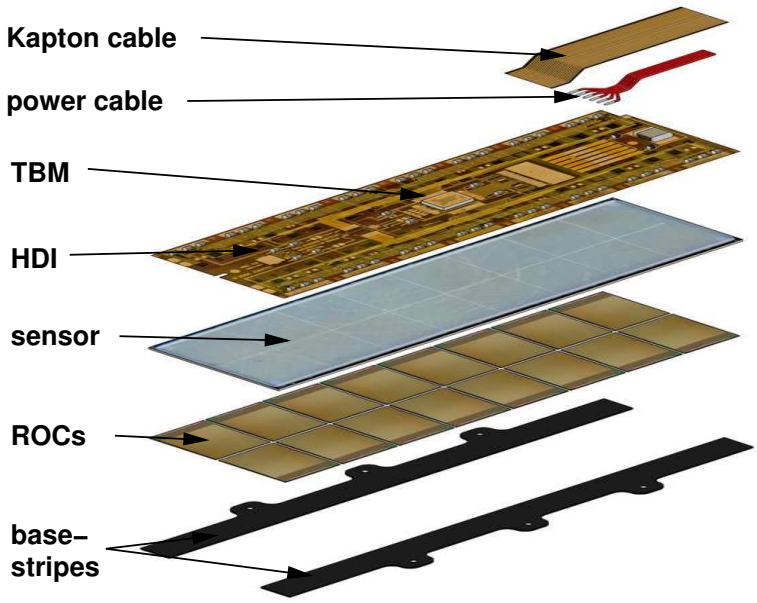

Figure 3.2: The final module for the barrel of the pixel vertex detector consists of the Kapton cable, the power cable, the High Density Interconnect, the sensor, the 16 readout chips and the base stripes.

the barrel part of the pixel vertex detector, because at the Paul Scherrer Institut (PSI)[1] only this part will be assembled. Module refers always to a full module, because all investigations mentioned in this work are done with a full module. The pixel vertex detector forward disks are in the responsibility of the US CMS Forward Pixel collaborators [41].

3.1 Components of the Module

The main components of a module are the Kapton®[2] cable, the power cable, the High Density Interconnect (HDI) with the Token Bit Manager (TBM) chip and other passive devices, the sensor, the 16 Readout Chips (ROCs) and the base stripes (Fig. 3.2) [42]. The overall size of the module is 66.6 mm $\times$ 26 mm. It has 66560 pixels and the weight is about 2.2 g without cables and approximately 3.5 g including both the Kapton and the power cable. The power consumption of one module is about 2 W, which corresponds to 125 mW per ROC and nearly 30 µW per pixel respectively. About 800 barrel modules including the half modules will be assembled at PSI. Therefore the module assembling is optimized for the mass production. It is described in detail in Reference [43].

[1] Paul Scherrer Institut, Villigen PSI, CH-5232 Villigen, Switzerland
[2] Kapton is a polyimide film and a registered trademark of DuPont.

3.1.1 Kapton Cable

The Kapton cable transmits the control signals from the printed circuit board which is mounted on the end-flange structure to the module. Furthermore it brings the analog information from the module to the end-ring print. Most of the signals are transmitted differentially by the Kapton cable which has 21 traces. To suppress crosstalk a solid copper layer is placed on the backside of the cable. Between sensitive pairs of lines like the analog signal and the trigger signal a line on ground potential is inserted. The signal cable is glued on the HDI and connected by wire-bonds. The impedance[3] is matched to the output impedance of the Token Bit Manager chip to minimize reflections from the cable. The stripline impedance is about 40 Ω. The pitch is 300 µm with a trace width of 190 µm. To reduce the amount of material, the thickness of the cable is 170 µm, which is the minimal allowed thickness for the connector used on the end-ring print. The chosen design of the signal cable allows cutting at any length according to the final position of the module on the carbon fiber (Sect. 2.4.2).

3.1.2 Power Cable

The power cable provides the module with the analog, digital and bias voltage. Additionally the corresponding ground potentials are transmitted. Therefore it consists of six isolated copper coated aluminum wires with a diameter of 250 µm each. The six wires are laminated to a flat power cable which is soldered to the HDI. The other end is equipped with a small printed circuit board which fits to the connectors on the end-ring print.

3.1.3 Token Bit Manager Chip

The Token Bit Manager chip [44, 45] is a custom, mixed-mode, radiation-tolerant integrated circuit that controls the programming and readout of a group of ROCs. The TBM will be glued on the HDI and connected by wire-bonds. The principle functions of the TBM include the following:

- It distributes the Level-1 Trigger (L1T) and 40 MHz clock to the ROCs.
- It controls the readout of the ROCs by initiating a token pass for each incoming L1T.
- On each token pass, it writes a header and a trailer word to the data stream coming from the ROCs.
- The header contains an 8-bit event number and the trailer contains 8-bits of error status. These 8-bits are transfered in 4 clock cycles as 2-bit analog encoded digital signal.
- Each arriving L1T will be placed on a 32-deep stack awaiting its associated token pass. Any subsequent L1T will be queued on the stack while the readout being busy with the previous event. Normally the stack will be empty. It is needed to accommodate high burst rates due to either noise, high track density events or trigger bursts. When the

[3]The impedance of a circuit element is defined as the ratio of the phasor amplitude across the element to the phasor current through the element. In the case of an ideal cable the impedance is $Z = \sqrt{L/C}$. Impedance mismatch results in signal loss and reflections.

stack is half full (16 pending triggers) the TBM will stop sending L1T signals to the ROCs but it will continue sending packet headers and trailers to the Front-End Driver in order not to loose synchronization.

The TBM contains a communication component called HUB. It serves as a port addressing switch for control commands sent from the Front-End Controller to the modules. There are four external ports on each HUB for communicating with the ROCs. In addition there is one internal port for communication with the TBM itself. Therefore each command will have a HUB address (5 bits) and a port address (3 bits) followed by the address of a ROC. The HUB address is defined by wire-bonds on the HDI. Actually the HUB address is the module address.

The TBM has two modes of operation: single mode and dual mode operation. This feature is related to the readout scheme of the pixel detector modules (Sect. 2.4.3 and Sect. 3.4). The modules of the inner two layers require two TBMs per module, each controlling 8 ROCs, since these modules are read out by two analog optical links. The two TBMs are configured by software in physical one TBM chip which is operated in dual mode. Therefore the two TBMs are addressed by one HUB and the same digital optical link, but read out by two analog links. The modules of the third layer are operated with a TBM in the single mode. In this case the TBM controls 16 ROCs.

3.1.4 High Density Interconnect

The High Density Interconnect (exact identification HDI_V3) is a low mass, flexible printed circuit board. It distributes the control signals and the power from the Kapton cable respectively the power cable to the ROCs and the TBM. The HDI is realized in a three metal layer design. The thicknesses of the layers in the sandwich structure are from top to bottom: 10 µm Kapton for isolation, 8 µm copper, nickel and gold, 10 µm Kapton, 6 µm copper and nickel, 10 µm Kapton, 6 µm copper and nickel and 14 µm Kapton. The top and middle layer are used for routing of the signals. The maximal trace length is about 40 mm and hence termination of signals is not an issue for 40 MHz signals. The traces act as pure capacitive loads (trace-ground capacity: about 3 pF/cm) and generate a timing skew. This load has been taken into account in the design of the output drivers of the ROC and TBM. To keep the relative phases constant for all control signals (40 MHz clock, L1T, reset) the traces of the different branches have equal capacitive loads. The third layer is used for the power distribution. It is designed as a grid structure to lower the coverage of the area with metal to about 50 %. The basic grid cell is equivalent in shape to the sensor pixel cell. Therefore the grid provides the possibility to inject charge to the sensor through the HDI by a laser for testing reasons. The HDI is equipped with passive components like capacitors for decoupling the power of the ROCs, a low pass filter for the sensor bias voltage and the TBM for controlling and reading out the module. After assembling the components, the HDI is glued onto the backside of the sensor. The ROCs will be connected by wire-bonds. Their addresses are defined by the layout of the HDI which simplifies the bonding. The ROC addresses are 0-15 and each group of 4 ROCs form a branch which is controlled by a separate external port of the TBM.

Beside the functionality of the HDI the design is optimized for a low mass contribution to the material budget of the module. Other design issues have been the optimization of

the yield. Therefore the distance between the traces was increased compared to former HDI versions. All contacts have been replaced by double contacts. Instead of the grid structure beneath the contacts a solid metal layer was designed to achieve a flat topology. To provide a good testing capability test pads for control signals have been placed. To improve the wire-bonding reliability and the rebonding possibility large bond pads were designed.

3.1.5 Sensor

The dimensions of the module sensor are 66.6 mm × 18.6 mm. One module sensor is segmented into 66560 pixels. To achieve a good spatial resolution in z-direction and in r-ϕ-direction an almost squared pixel shape was adopted. The pixels have a size of 100 µm × 150 µm ($r\phi \times z$) to match the pixel size of the ROCs. The distance between pixels from different ROCs is larger than between pixels of the same ROC. To avoid insensitive regions the sensor pixels along the ROC boundaries have twice the area. The pixels at the ROC corners have the fourfold size. The thickness of the sensor is 285 µm ± 15 µm. The detailed design and the performance of the sensor is described in Section 3.2.

3.1.6 Readout Chip

The most important parts of the modules are the 16 ROCs. The final ROC which will be used for the mass production of the modules is the PSI46V2. The physical size of the PSI46V2 is 9.8 mm × 7.9 mm. To reduce the contribution to the material budget of the module (Sect. 3.3), the wafers with the ROCs are ground from 750 µm to 175 µm. The ROCs are connected to the readout and control electronics by wire-bonds to the HDI. The HDI distributes also the power to the ROCs. The number of pixel unit cells per ROC is 4160 with a pixel size of 100 µm × 150 µm. Each pixel unit cell is connected to the corresponding sensor segment via an indium ball. The ROC used for the barrel modules is also used for the forward disks. The architecture of the final pixel detector readout chip is described in more detail in Section 4.

3.1.7 Bump Bonding

The sensor and the readout chips are connected by a dedicated bump bonding technique. Since the pitch is below 100 µm, no standard industrial process is available. Therefore a bump bond process was developed at PSI as a part of the R&D for the CMS pixel detector. The indium bumps in this process have a diameter of about 20 µm (Fig. 3.3 and Fig. 3.4). For more information about the developed bump bonding process see Reference [46].

3.1.8 Base Stripes

The base stripes are needed for mechanical stability and for mounting the module on the cooling structure. The outline of the base stripes is 65 mm × 26 mm. The initially planed solid silicon base plate was replaced by two single stripes of 250 µm thick silicon nitride (Si_3N_4) to reduce the amount of material. Si is perfect CTE[4] matched but vulnerable to cracking.

[4] CTE = Coefficient of Thermal Expansion

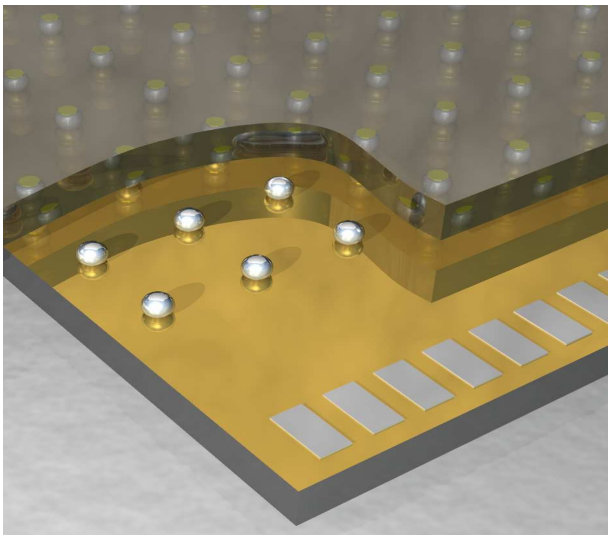

Figure 3.3: Schematic view of a bump bonded hybrid consisting of the sensor and the readout chip.

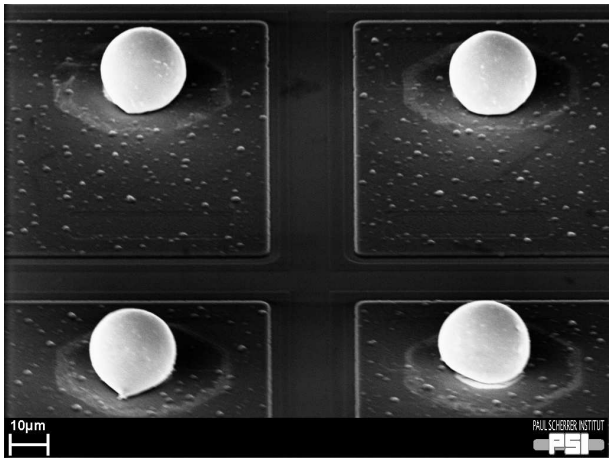

Figure 3.4: A scanning electron micrograph of the indium bumps on the sensor. The distance between the bumps is 100 µm and the bumps have an diameter of about 20 µm [46].

Si_3N_4 has a five times higher fracture toughness and is CTE matched to silicon, too. Otherwise thermal stress would shear off the ROCs from the sensor. Since the filter capacitors of the ROCs have been moved from the base plate to the HDI no electrical circuitry on the base stripes is needed anymore. This is a benefit concerning the material budget and it lowers the cost of the base stripes since no photo-lithographic processing of the base stripes is required.

3.2 Silicon Sensor for the Modules of the Pixel Detector

The sensors of the pixel detector must survive fluences up to 6×10^{14} n_{eq}/cm^2 corresponding to the first four years of LHC operation for the innermost pixel layer. The harsh radiation environment will determine the silicon sensors behavior and is therefore the main concern. The pixel detector will be operated at -10 ℃ to suppress the increasing leakage current with ongoing irradiation (Sect. 4.2.1). Even in the not data taking period the temperature of the sensor will be -10 ℃ to prevent reverse annealing[5].

[5] Observing a radiation damaged detector after the end of the irradiation process, one notices that the observed damage to the detector diminishes with time. The rate of damage decrease is strongly dependent on the temperature at which the detector is kept during waiting period. This observation can be naively interpreted as a partial disappearance of radiation generated crystal defects and was called "annealing". But in many cases defect complexes may just be transformed into other more stable defect types with changed properties. As new defect complexes are produced, the effect of annealing may not always be beneficial for detector performance. An example of such a detrimental effect is the increase in space charge after initial annealing. This effect has been called "reverse annealing" [47].

3.2.1 Induced Charge and Radiation Dose

Charged particles traversing material lose a part of their energy through elastic collisions with electrons. With the Bethe-Bloch equation [3] one can calculate the ionization energy loss dE/dx also called stopping power in dependence of β the velocity of the traversing particle (units of dE/dx: MeV cm^{2}g^{-1}). By doing this, one gets the deposited energy by multiplying dE/dx with the density of silicon and the thickness of the traversed material. Concerning dE/dx, there are two simplifications for all practical purposes in high-energy physics: in a given material dE/dx is only a function of β. Most relativistic particles have energy loss rates close to the minimum of the Bethe-Bloch equation. They are said to be Minimum Ionizing Particles (MIPs). For silicon the density is 2.33 g/cm^3 and the thickness of the pixel detector sensor is 285 µm. A MIP deposits therefore 1.70×10^{-14} Joule which corresponds to about 29000 e$^-$. Results from measurements are about 23000 e$^-$ for one MIP[6] [49]. The difference between the theory and the measurement is caused by the fact, that the former gives the mean value and the latter the most probable value of the Landau distribution [50]. This distribution describes the energy loss of charged particles passing through a thin layer of matter. For the conversion of particle fluences to radiation dose one has to multiply the number of particles with the ionization energy loss of a traversing particle for the corresponding sensor material and thickness. By doing this one gets the total deposited energy per area, which can be normalized to a certain amount of material by dividing with the density and the thickness of the material. For a MIP of 29000 e$^-$ (23000 e$^-$) one gets 4×10^{14} n$_{eq}$/cm^2 (5×10^{14} n$_{eq}$/cm^2) which is equal to about 100 kGy.

3.2.2 Design

The pixel detector will be equipped with n-in-n type silicon sensors (Fig. 3.5). The pixels are formed by n^+ implants on n bulk silicon. The backside is made of a p^+ type silicon layer. Electron collection has the advantage that after irradiation induced type inversion[7] [51] of the substrate, the highest electric field is located close to the collecting electrodes. This ensures operation of partly depleted sensors which might be necessary after type inversion due to the subsequent decrease of the depletion depth and the active sensor volume. The double-sided processing of these devices allows the implementation of guard rings only on the p-side of the sensor. The 16 guard rings are made to gradually drop the potential between the front and back surface of the sensor. They keep all sensor edges at ground potential. The design of the guard rings has been optimized in the past [52]. In order to detect the signal on the n^+-implants the sensor inter-pixel isolation has to be provided. Since there is a conductive interconnection between the pixels caused by electron accumulation close to the sensor surface. Due to the superior performance after irradiation and the possibility to

[6] In semiconductors, only part of the energy loss is used for the creation of electron-hole pairs. In silicon the average energy used for the creation of a pair is 3.62 eV, three times larger than the band gap of 1.12 eV. The rest of the energy is used for the creation of phonons (lattice vibrations), which means finally thermal energy. This is true for radiation energies that are large with respect to the band gap [47, 48].

[7] The effective doping of an initially n-type silicon decreases with irradiation and then the material becomes intrinsic at an irradiation fluence of a few times 10^{12} n$_{eq}$/cm^2. Above this value the doping becomes effectively p-type ("type inversion") and rises linearly with the fluence. The fluence at which type inversion occurs depends on the original doping.

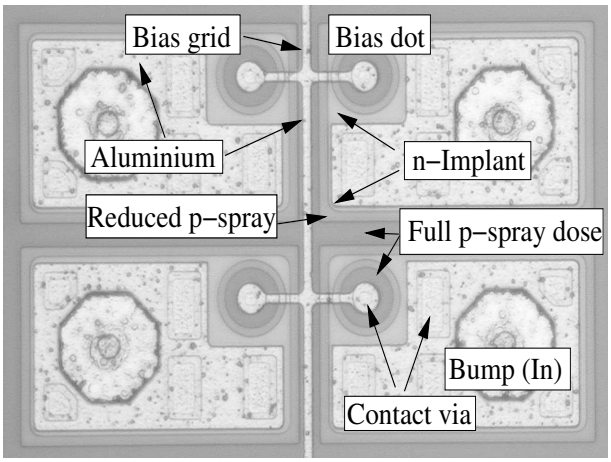

Figure 3.5: Pixel layout of the sensor designed in p-spray technique with punch through structures and a bias grid.

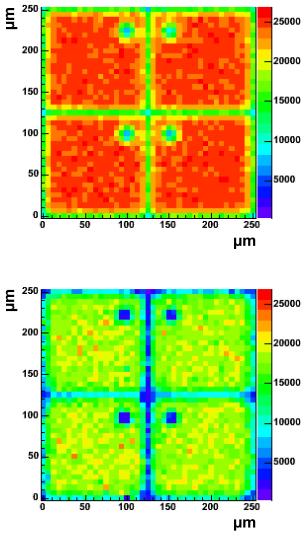

Figure 3.6: Charge collection of the p-spray sensors before irradiation (upper Figure) and after irradiation with 6.7×10^{14} n_{eq}/cm^2 (lower Figure) over the pixel surface at full depletion. Red (blue) corresponds to high (low) charge levels in electrons.

implement a bias grid, the moderated p-spray technique was chosen. The isolating moderate boron spray concentration of p-impurities is performed without a photo-lithographic mask and therefore no structuring is possible. The bias grid is connected by a small punch through structure to each n^+ implant [53]. They allow wafer current-voltage (IV) measurements before bump bonding the ROCs to the sensor. In addition the bias grid keeps accidentally unconnected pixel cells close to the ROC potential. This is important to prevent discharging in air, especially when sensors are operated at a high bias voltage. The post irradiation behavior is improved by using Diffusion Oxygenated Float Zone (DOFZ) material [54]. It has a resistivity of 2-5 kΩcm.

3.2.3 Performance

To investigate the performance of the sensors with ongoing irradiation samples were irradiated up to a fluence of 10^{15} n_{eq}/cm^2 with 24 GeV protons from the CERN PS. The sensors with pixel dimensions of the former design (125 µm × 125 µm) were bump-bonded to an earlier readout chip (PSI30). The samples were tested with 150-225 GeV pions in the H2 beamline of the CERN SPS in 2003 and 2004 [31, 32]. The beam test setup consisted of a beam telescope [55] made of 8 silicon microstrip detectors (4 measuring the horizontal x and 4 the vertical y impact points) with 50 µm readout pitch and a fast trigger diode. The hit coordinates on the sample, which was mounted between the telescope planes on a tiltable and cooled support, could be determined from the telescope with a resolution of $\sigma \sim 1$ µm. The entire setup was operated in a 3 T magnetic field parallel to the beam to measure the Lorentz angle and

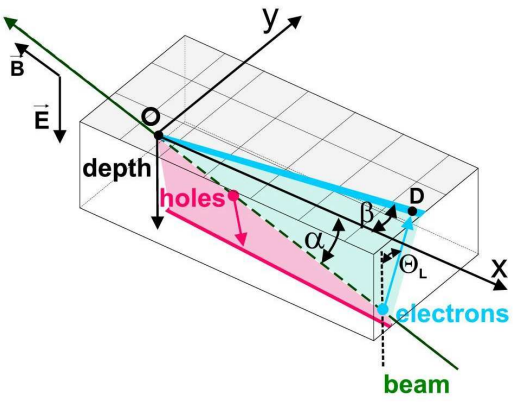

Figure 3.7: Lorentz angle Θ_L measurement with the grazing angle method.

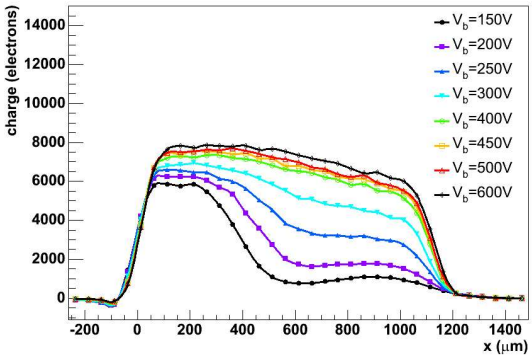

Figure 3.8: Collected charge signal as a function of x for p-spray sensors exposed to a fluence of 6×10^{14} n_{eq}/cm^2 for various bias voltages.

perpendicular to the beam to investigate the position resolution.

3.2.3.1 Charge collection

In the beam test it was possible to scan the surface of the sensors with the telescope to determine the charge collection efficiency. Irradiated sensors show trapping of charge carriers. The radiation changes the electric field strength value in the silicon bulk and introduces charge trapping centers which are crystal defects. This leads to the degradation of the charge collection efficiency caused by trapping. Trapping is the capture of an electron by a trapping center and after some time the electron is emitted again. In addition the induced signal is reduced by incomplete depletion of the sensor volume. Both effects can be decreased by increasing the sensor bias. Therefore the sensor design must allow the operation at high bias voltage without electrical breakdown. For the pixel detector a maximal value of 600 V is foreseen. In the beam test the bias voltage was increased from 100-600 V to reach full depletion. Figure 3.6 shows the average charge collected for a p-spray sensor before and after irradiation with 6.7×10^{14} n_{eq}/cm^2. The charge collection efficiency is lower in the punch through regions. The irradiated sensors have a particle detection efficiency of 99 % with a threshold of 2000 electrons.

The charge collection depends on the location of the charge deposit in the sensor bulk. To study the charge collection in dependence of the depth the grazing angle method was used. Therefore high energy pions traverse the sensor at an angle $\alpha = 15°$ with respect to the pixel surface (Fig. 3.7). The pixels at the distance x from the impact point along the beam direction sense the charge deposit at a depth $d = x \tan \alpha$. Figure 3.8 shows the average signal as a function of x for various bias voltages and for a fluence of 6×10^{14} n_{eq}/cm^2. The depletion is believed to start from the implant side after irradiation leading to type inversion. Thus charge should be collected only from the depletion region close to the pixel implant at low bias voltages. However, the measured dependence of the charge collection efficiency indicates that even at low bias voltages the charge is collected from both sides of the sensor. This means

that for the irradiated sensors the depletion starts from both sides of the sensor bulk. This observation is supported by the direct measurement of the electric field in the sensor bulk [32] and by a detailed simulation. The behavior of irradiated sensors does not correspond to the classical picture of a partially depleted sensor, but can be described by a double junction model [59, 56, 57]. A detailed modeling of charge collection in heavily irradiated sensors was performed and tuned to the test results for the 125 µm × 125 µm sensor pixel. Based on this the simulation program PIXELAV [58] can be applied to the final pixel dimensions of 100 µm × 150 µm as well.

3.2.3.2 Position resolution

To improve the spatial resolution of the pixel sensor analog interpolation between neighboring pixels will be performed. The Lorentz deflection in r-ϕ-direction caused by the magnetic field and the drift direction of the electrons and holes along the electric field lines is used to distribute the induced charge over two and more pixels[8]. The resolution along the z-direction is determined by the pixel pitch in the region with low pseudorapidity ($\sigma = \text{pitch}/\sqrt{12} \Rightarrow \sigma_z = 43.3$ µm)[9]. For tracks hitting the sensor at an inclined angle, the resolution is improved by charge sharing.

For investigating the position resolution in the beam test the 3 T magnetic field was perpendicular to the incident beam to reproduce the situation of $\eta = 0$ in the pixel detector barrel. The position resolution was measured with various samples irradiated up to a fluence of 9.7×10^{14} n_{eq}/cm^2. Due to the width of the flat modules (~ 18.6 mm) the spatial resolution along the r-ϕ-direction will vary with ϕ. The measured charge sharing was simulated with PIXELAV (Sect. 3.2.3.1) and afterward the charge sharing for the 100 µm × 150 µm pixel and the CMS 4 T magnetic field were predicted. The result is shown in Figure 3.9 for $\phi = \pm 10°$ corresponding to the innermost layer (radius 44.4 mm). It lies between 10 µm and 20 µm, depending on the irradiation fluence and polar angle. After the first four years of operation the resolution at the innermost barrel layer is still below 20 µm along the r-ϕ-direction and depends weakly on the polar angle [32]. The resolution along the z-direction is better than 20 µm. The spatial resolution can be improved by using the η correction [60]. Applying this correction on charge collection profiles simulated with PIXELAV spatial resolutions below 15 µm can be achieved for irradiated sensors [61].

[8] $\vec{F}_L = q\vec{v} \times \vec{B}$ with $\vec{v} = \mu \cdot \vec{E}$; μ is the mobility of the charge carrier in silicon. It depends on the field strength and hence cause a velocity saturation [47].

[9] The precision of the position measurement for segmented sensors depends mainly on the strip/pixel spacing. As long as only digital information is used (taking the center position of the strip as the measured coordinate) and the effects arising from track inclination and charge diffusion during collection can be neglected, the measurement precision (root-mean-square deviation from the true coordinate) is given by the strip/sensor pitch p as:

$$\langle \Delta x^2 \rangle = \frac{1}{p} \int_{-\frac{p}{2}}^{\frac{p}{2}} x^2 dx = \frac{p^2}{12} \tag{3.1}$$

The measurement precision is substantially improved with analog readout if the pitch is chosen small enough. The signal charge - due to diffusion - is collected on more than one strip and the coordinate is found by interpolation, e.g. by calculating the center of gravity using the single pixel signal charges.

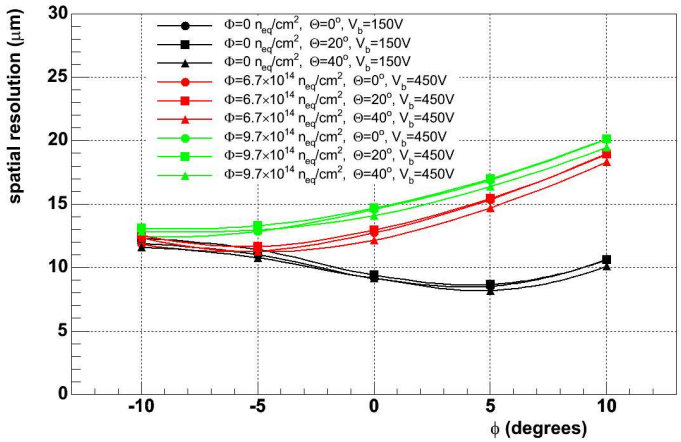

Figure 3.9: Predicted r-ϕ-position resolution in the CMS pixel detector barrel as a function of the azimuthal angle ϕ, for various polar angles Θ and irradiation fluences.

3.2.3.3 Lorentz angle

The deflection angle (Lorentz angle Θ_L) as a function of depth in the 3 T magnetic field was investigated with the technique described in Reference [52, 62]. Therefore the magnetic field was parallel to the beam, which enters the sensor plane at the grazing angle α. Without magnetic field the charge generated at a given depth d would reach the pixel at a distance x along the beamline (Sect. 3.2.3.1). With a magnetic field the charge is deflected towards the adjacent pixel rows. Hence the measurement of the charge distribution among adjacent pixels yields the Lorentz angle Θ_L as a function of x and the sensor depth [63]. Figure 3.10 shows the typical displacement of the collected charge at the surface of the sensor. In Figure 3.11 the displacement of the charge as a function of the depth at which the charge was produced for various irradiation levels is shown. The displacement and thus Θ_L decreases with irradiation since the bias voltage was increased to achieve full depletion. The extrapolated Lorentz angle for a 4 T magnetic field is for the unirradiated sensor with a bias voltage of 100 V $(26.3 \pm 0.8)^\circ$ and $(11.6 \pm 1.4)^\circ$ after a fluence of 6.7×10^{14} $\mathrm{n_{eq}/cm^2}$ (450 V bias).

3.2.3.4 Measured performance

The position resolution of the p-spray pixel sensor is measured to be about 10 to 20 µm for the r-ϕ-direction depending on the radiation dose and the polar angle. After irradiation with 6×10^{14} $\mathrm{n_{eq}/cm^2}$ the resolution is still better than 20 µm. The spatial resolution in z-direction varies in the range from 20 µm to 40 µm and weakly depends on the irradiation dose. The Lorentz angle is for the unirradiated sensor about 26° and after a fluence of 6×10^{14} $\mathrm{n_{eq}/cm^2}$ it is about 11.6°. The breakdown voltage exceeds by safely the required value of 600 V.

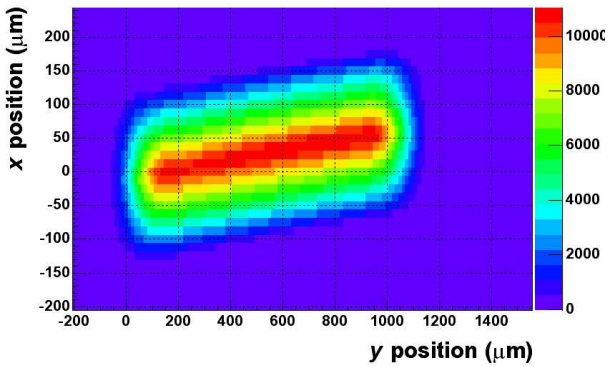

Figure 3.10: Deflection of the induced charge in a 3 T magnetic field measured with the grazing angle method. The beam enters the sensor from the left.

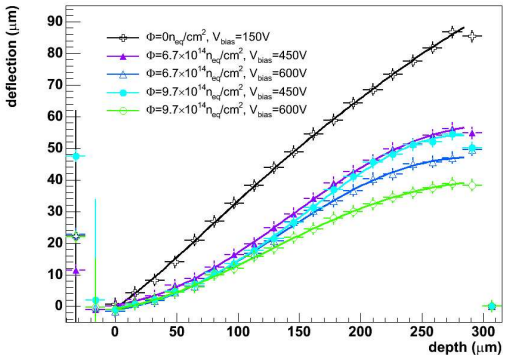

Figure 3.11: Charge deflection at the surface as a function of the depth at which the charge was produced for sensors irradiated with different fluences.

3.3 Material Budget of the Module

The Material Budget (MB) is a crucial issue concerning the error of the Impact Parameter (IP) determination. In Section 2.4.4 by means of a simple straight line fit it is derived that for a muon with a transverse momentum of 2 GeV the contribution to σ_{IP} is dominated by multiple scattering. The material of the pixel detector layers cause multiple scattering. The MB for the entire pixel detector with three layers is described in Section 2.4.5.1. The distribution of the material is shown in Figure 2.21 and Figure 2.22. The breakdown of the contribution to the MB of the pixel detector for different module components is charted in Figure 3.12. The amount of material of each component is smeared over the entire area of the module. Hence the plot is independent of η and ϕ. The graph represents the MB for a module without any mechanical support structure. Each sector is labeled with the component and its contribution in percent relative to the total MB of the module. The absolute MB of all module components without support structure sum up to 1.2 % of one radiation length for $\eta = 0$ [33]. The 1.2 % are the result of an enormous effort made to reduce the MB. The Kapton cable has the smallest pitch and thickness allowed to use commercial connectors on the end-flange print; the layers of the HDI are thin and have partly grid structure to lower the metal coverage; the number of SMD components was reduced by a factor of about 2 compared to former designs and the size of the devices is the smallest available (e.g. 1 μF $\simeq 1 \times 0.5 \times 0.5$ mm^3); the ROCs are thinned down; the sensor thickness is related to the induced charge and therefore not reducible; the solid baseplate was replaced by two base stripes without any metal layer. In Figure 3.13 the MB of a module including the mechanical support structure is shown. The aluminum tubes and the coolant (C_6F_{14}) are the dominant parts of the support structure. The MB of the module including the mechanical structure sums up to 1.6 % of one radiation length.

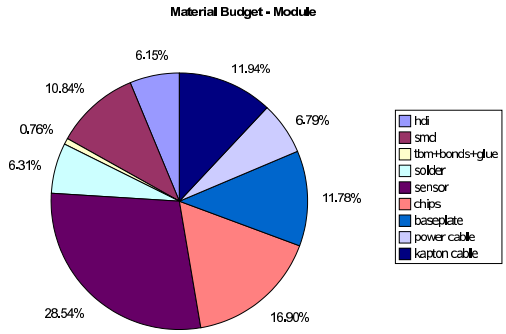

Figure 3.12: Material budget of a barrel module without any mechanical support structure. The total MB of all module components sum up to 1.2 % of one radiation length [33].

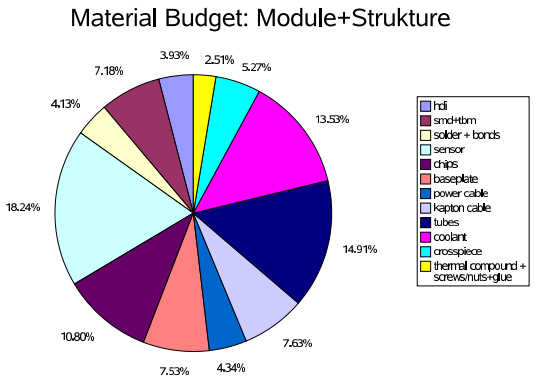

Figure 3.13: Material budget of a barrel module including the mechanical support structure and coolant. The total MB of all module components is 1.6 % of one radiation length [33].

3.4 Readout and Control Scheme

The pixel detector readout and control system between the electronics room and the modules is described in Section 2.4.3. According to Figure 2.18 the control chain provides the modules with the 40 MHz system clock, the I^2C programming signals and the Level-1 Trigger (L1T) signal. The I^2C protocol requires two signals: clock and programming data. Since the modified I^2C protocol works with 40 MHz, the system clock for the operation of all front-end devices is used for the I^2C programming too (Fig. 3.14). The HUB passes the command stream unmodified to the ROCs and the corresponding TBM after stripping off the HUB and port address. For control reasons the clock and the command stream is reflected to the control chain [64]. CMS requires that two subsequent triggers are separated by at least 2 clock cycles (75 ns from edge to edge of the trigger pulse). This provides the possibility to use the 2 additional clock cycles to encode other control signals. In total there are 4 different control signals on the L1T signal: Reset only the ROCs [111], reset the ROCs and the TBMs [101], the "real" L1T signal [110] and the precal signal. It is used to send a calibration signal to the ROCs [100] out of the beam-time periods. The L1T and the system clock are distributed by the TBM in parallel to the 4 branches. Each branch consists of 4 ROCs (Fig. 3.14 and Sect. 3.1.3). The TBM controls the readout of the ROCs by initiating a token pass for each incoming L1T. If the token signal leaves the TBM, the header word appears on the analog output. The header is followed by the data stream of the ROCs. The ROCs are read out serially. After the token has entered the first ROC the double columns are initiated to put consecutively their hits to the corresponding L1T on the analog out. The token goes on to the next ROC when all double columns finished. After the arrival of the token in the TBM, the trailer word is attached to the data. The number of ROCs passed by the token depends on the mode the TBM is operated. In the single mode 16 ROCs are passed and in the dual mode 8 ROCs are served by the token. The analog data are transmitted by the analog chain to the data acquisition system. For more details concerning the readout and control system

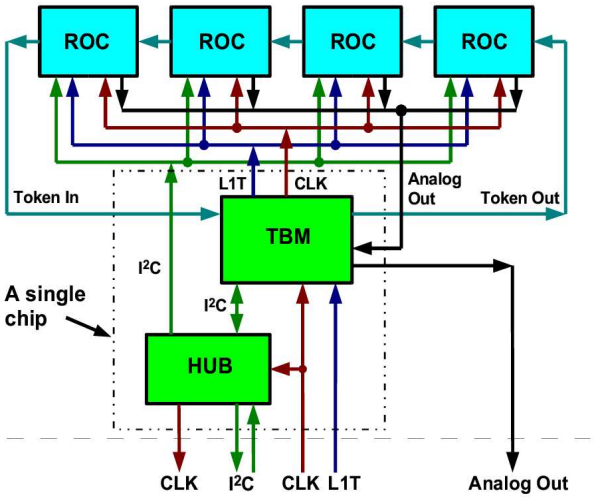

Figure 3.14: Module readout and control scheme. 4 ROCs are controlled by an external port of the TBM. The HUB and the TBM are in one single chip.

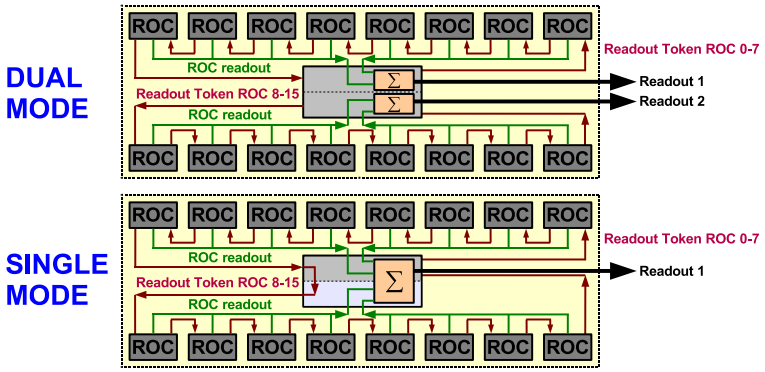

Figure 3.15: Token passage for single and dual mode operation of the TBM on the module.

see Reference [21].

The control system has to download the large number of parameters to the front-end chips, the TBMs and the ROCs. The TBM has 11 8-bit DACs and registers. With the total number of about 800 TBMs for the barrel part of the pixel detector about 9 kByte of data will have to be downloaded. Each ROC has about 27 8-bit DACs and registers (Sect. 4.1.3). The total number of about 11500 ROCs results in about 300 kByte for downloading. However, the dominating part of data for downloading arises from the programmable fine adjustment of the pixel threshold. Therefore each pixel contains 5 bits (Sect. 4.1.1). For 48×10^6 pixels the data volume sum up to about 48 MByte. The described control system with 64 parallel control networks and the 40 MHz clock can download the full amount of data in about 30 s. The limiting factor is the VME bandwidth limitation since all the programmed parameters have to be downloaded from the control PCs to the VME front-end controller units (Sect. 2.4.3).

3.5 Summary

The three layers of the barrel part of the pixel detector are composed of about 800 modules. The main components of the modules are the 16 Readout Chips (ROCs) and the sensor. The ROCs, produced in a 0.25 µm process, are thinned down to 175 µm. They are bump bonded to the n-in-n type silicon sensors, with a thickness of 285 µm. The position resolution of the p-spray pixel sensor is 10 to 20 µm for the r-ϕ-direction depending on the irradiation. The spatial resolution in z-direction is in the range of 20 to 40 µm. The control signals are transmitted to the module by a low mass fine pitch Kapton cable. The analog, digital and bias voltage are provided by a laminated flat cable. The distribution of the control signals and the power on the module is performed by the High Density Interconnect (HDI). The HDI is a flexible, low mass, fine pitch printed circuit board. It is equipped with passive components and the Token Bit Manager (TBM) chip which organizes the readout of the module and distributes the control signals. For mechanical stability the module has two base stripes of Si_3N_4 250 µm thick. The overall dimensions of the module are about 66.6 mm $\times$ 26 mm. It is segmented in 66560 pixels and has a power consumption of about 2 W (approximately 30 µW/pixel). The material budget of the module is without support and cooling structure of a layer about 1.2 % and with support structure 1.6 % of one radiation length X_0. The total weight of a module is 2.2 g without cables and 3.5 g including the cables.

Chapter 4

Readout Chip of the Pixel Vertex Detector

4.1 Readout Chip

The bunch crossing frequency at the Large Hadron Collider will be 40 MHz. At high luminosity operation every 25 ns two bunches with about 10^{11} protons each are colliding. For every bunch crossing the average number of 20 inelastic *pp* collisions will happen. The rare interesting events are superimposed on top of these minimum bias events. According to simulations about 1000 tracks will emerge from the interaction point every 25 ns. Since the innermost layer of the pixel detector is at a radius of 44.4 mm, the track density will be 40 MHz/cm^2 at high luminosity (10^{34} cm^{-2}s^{-1}). The number of tracks per cm^2 is in the region of the pixel detector increased by the 4 T magnetic field of CMS. The Level-1 Trigger (L1T) rate will be up to 100 kHz and the trigger decision is taken within a latency of 3.2 µs corresponding to 128 bunch crossings (more details in Chap. 2). During the latency the readout chip must store locally the pulse heights, the addresses and the bunch crossing numbers of the hit pixels. Because of inclined tracks and Lorentz drift of the induced signal charge in the 4 T magnetic field several pixels might be hit by a single track forming a hit cluster. The analog pulse height information is needed to improve the accuracy of the position reconstruction for clusters by signal interpolation (Sect.3.2.3.2). About one per 8000 of the events will be selected[1]. If an event is confirmed by the L1T only the pixels with a hit are read out. Zero-suppression is crucial due to the large number of about 60×10^6 channels of the entire pixel detector. Not confirmed events will be discarded in the ROC after passing the latency. To be sensitive for rare decays dead-time must be as little as possible. Therefore continuous data taking and simultaneous readout operation is required. A granularity of the order of 100 µm is necessary for successful pattern recognition and a good position resolution (Sect. 2.4.4). The high granularity reduces also the pixel occupancy. The resulting high density of 6500 pixels per cm^2 limits the acceptable power dissipation per channel to a few microwatts. The high track density of 40 MHz/cm^2 which corresponds to 6×10^{14} n_{eq}/cm^2 respectively about 100 kGy per year have to be survived by the pixel detector without any unacceptable degradation in

[1] 20 minimum bias events per bunch crossing become 800×10^6 per second and with a L1T rate of 100 kHz one selects about 1 out of 8000 events.

performance. Therefore the ROC has to be designed in a radiation hard technology.

The development of the ROC started with the DMILL process (Durci Mixte sur Isolant Logico-Lineaire) [20]. DMILL is a special process developed for radiation hard devices. It is a Silicon On Insulator (SOI) BiCMOS process which offers complimentary MOS transistors as well as bipolar transistors. The circuits with a smallest feature size of 0.8 µm are processed on dedicated 6 inch SOI wafers. Two metal layers are available for routing. Therefore the number of transistors per pixel and the number of bus lines were limited. To avoid partly this limitation individually designed transistors have been necessary. The first prototype of the ROC, PSI43, with the complete functionality was fabricated in DMILL technology in 2002 [65]. Basically PSI43 worked as expected but insufficient rate capability for high luminosity operation at the inner layer was discovered. According to the CMS TDR [5] it was initially planned to operate at low luminosity layer 1 and 2 of the pixel detector. For high luminosity the operation of layer 2 and 3 was foreseen. The current planning of CMS is to operate the pixel detector at low and high luminosity with all three layers.

In order to improve the performance and the yield the ROC design has been translated into a commercial Deep Submicron (DSM) process available through a CERN frame contract. The process is a 0.25 µm bulk CMOS technology which is a well known commercial process also used by conventional chip industry. Therefore it is cheaper than DMILL. The Integrated Circuits (ICs) are fabricated on 8 inch standard wafers which results in more chips for the same number of processing steps. The number of processing steps are the dominating cost factor in chip production. Moreover a higher yield than with DMILL process was expected (PSI43 yield about 20 %). Another benefit of DSM is the lower power consumption. The power dissipation is about a quarter compared to DMILL since the supply voltages and the currents are lower. DSM CMOS technologies have been shown to provide sufficient radiation hardness when radiation-tolerant layout rules are followed [66]. These rules require e.g. ring gates and guard rings. The DSM process offers a smallest feature size of 0.25 µm and five metal layers for routing. With the resulting lower capacitive loads faster circuits are possible. Furthermore a higher device density is permitted which allows to design more complex circuits. The gain was partly compensated by the radiation hard layout rules. Finally the device density is about a factor of 3 higher in DSM compared to DMILL. The translation from the prototype ROC in DMILL technology to DSM process followed closely the architecture of PSI43. Besides some minor problems no reason was found for fundamental design changes. The size of the active area was not changed but the possibilities of the quarter micron process were used to reduce the data losses for high luminosity operation at the innermost layer (data losses are described in detail in Section 7.3). The number of pixels is increased from 2756 to 4160. The pixel dimensions changed from 150 µm $\times$ 150 µm to 100 µm $\times$ 150 µm. The size reduction was in the plane perpendicular to the magnetic field for the CMS pixel barrel and improves charge sharing between the sensor pixels. To decrease the data losses the number of data buffers and time stamp buffers were increased. Despite the increase of buffers the size of the ROC periphery was reduced which eases the assembly of the modules. To make the design process more efficient a library of standard cells was used. In DMILL many blocks had been optimized for layout space and device count. The first version of the ROC designed in DSM, PSI46V1, was received in august 2003. A summary of the chip parameters and a comparison to the DMILL chip are given in Table 4.1. Due to a design error in the readout logic, the

	PSI43	PSI46
Technology	DMILL (0.8 µm, SOI, BiCMOS)	0.25 µm bulk CMOS
Chip size	7.95×10.8 mm^2	7.9×9.8 mm^2
Transistors	430 k	1280 k
No. of pixels (columns × rows)	2756 (52×53)	4160 (52×80)
Pixel size ($r\phi \times z$)	150 µm × 150 µm	100 µm × 150 µm
Supply voltages	-4.5 V, -3.5 V, -2.5 V	2.5 V, 1.5 V
External capacitors	6	3
Total power dissipation (pixel)	500 mW (180 µW)	120 mW (29 µW)

Table 4.1: Parameters of the ROC PSI46 designed in 0.25 µm technology compared to the parameters of the PSI43 readout chip fabricated in the DMILL process.

analog pulse height of the pixel hits could not be read out correctly. Furthermore a parasitic feedback loop involving a gate capacitance acting in parallel in all pixels leads to oscillations of one of the voltage regulators. When the relevant node is stabilized externally with a capacitor, the chip can be operated without a problem. With these exceptions, the chip was fully functional. A high rate beam test to measure the efficiency under LHC like conditions as well as measurements with irradiated ROCs were performed. It performed well in the beam test and showed sufficient radiation hardness. For more details concerning the translation and test results of PSI46V1 see Reference [67]. The second iteration of the translated ROC, PSI46V2, contains small modifications compared to PSI46V1. It is the production version and described in the following paragraph.

The ROC PSI46V2 can be divided into 3 major blocks with different functionalities: the sensitive pixel array which is organized in double columns of Pixel Unit Cells (PUCs), the double column periphery which controls the readout and the trigger validation within double columns and a global part containing control and supply functions for the ROC (Fig. 4.1).

4.1.1 Pixel Array

The sensitive pixel array has in total 4160 pixels. The pixels are organized in 26 Double Columns (DCOLs) with 160 pixels each. Hence a ROC has 52 columns and 80 rows. The rows are in z-direction and the column are in r-ϕ-direction. The pixel size is 150 µm × 100 µm ($z \times r\phi$) see Table 4.1. The input of each pixel unit cell is connected to a sensor segment (pixel) by a indium ball of 20 µm in diameter. The PUC can be divided into an analog and a digital part. A schematic view of the PUC is shown in Figure 4.2. The PUCs are connected to the double column periphery by a bus structure, which is also shown in the schematic view on the right. The current signal from the sensor enters a two stage charge sensitive preamplifier and shaper system. Alternatively, calibration signals can be injected by two different methods: Directly to the amplifier input node through a 4.8 fF injection capacitor or indirectly by capacitive coupling through the air gap between a top metal plate in the PUC and the sensor pixel. The former mechanism can be used for various tests in the laboratory without incident particles available (Chap. 6) e.g. trimming the comparator threshold. The latter can be used for testing the bump bond connection [68]. A globally programmable current source at the

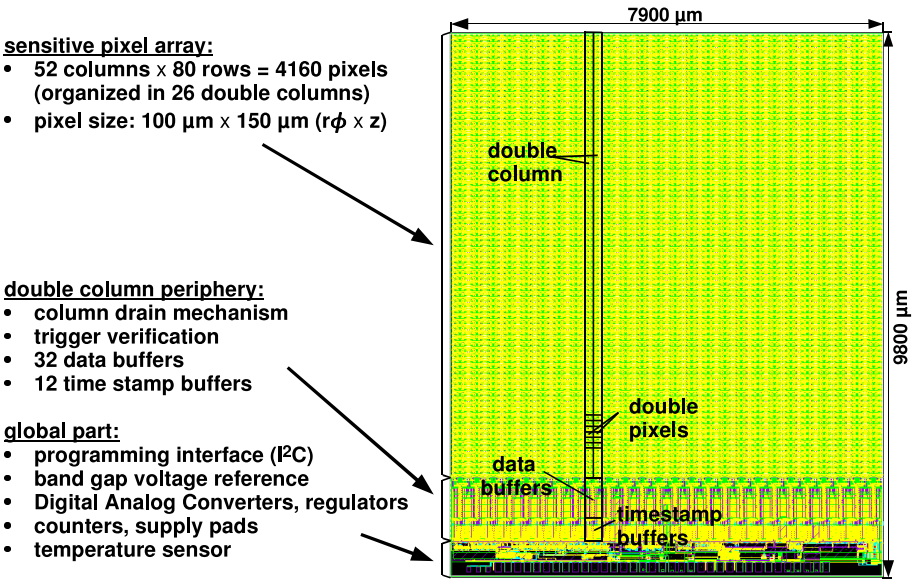

Figure 4.1: ROC layout with 3 major blocks: sensitive pixel array, double column periphery with control function within the double column and a global part with control and supply functions.

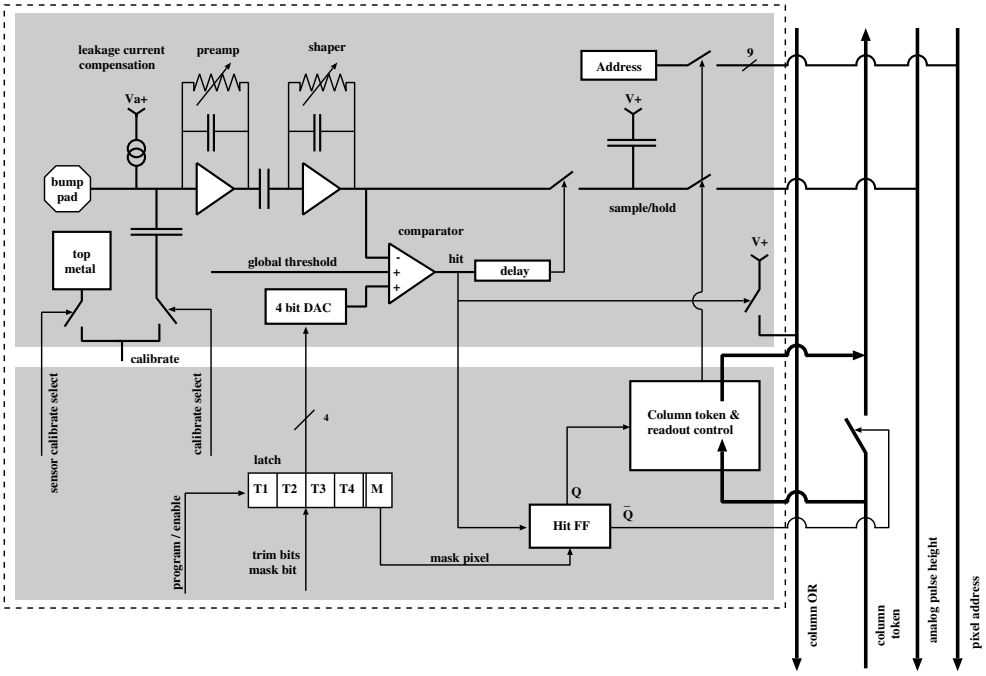

Figure 4.2: Schematic overview of the PUC. The PUC can be divided in an analog (top) and digital part (bottom). On the right the double column bus trace is shown.

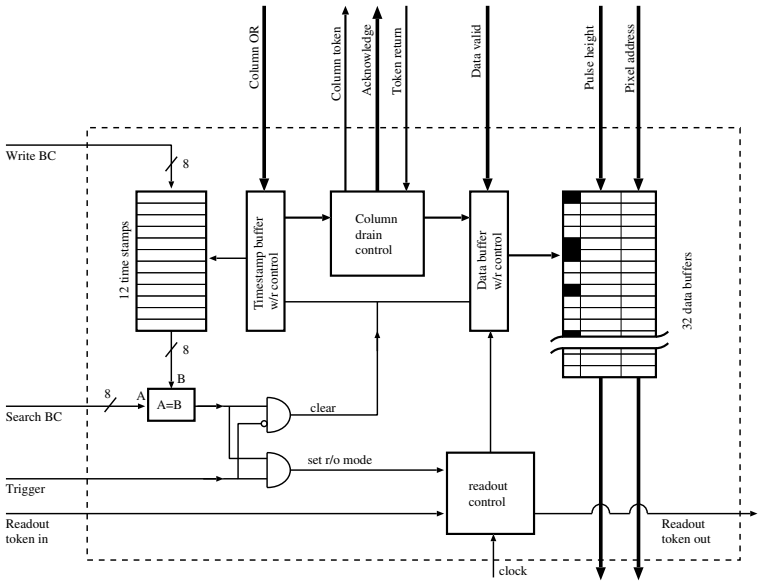

Figure 4.3: Schematic overview of the double column periphery.

input node will be used for compensation of the sensor leakage current. Since the leakage current is related to the pixel size, the strength of the current source is adopted to edge and corner pixels (Sect. 3.1.5). These pixels are larger than the regular ones. Investigations of the preamplifier and the shaper performance concerning the leakage current can be found in Section 4.2. Zero-suppression is performed with a comparator. A global threshold can be programmed for all pixels of a ROC. In order to compensate local transistor mismatch each pixel has 4 one-bit storage cells (called trim bits) connected to a 4-bit DAC (digital analog converter) to do a fine adjustment of the threshold. Furthermore a mask bit allows to enable or disable pixels. The used storage cells are protected against single event upsets (Chap. 5). Once the comparator is above threshold the shaper output signal is stored in a sample-and-hold circuit with an adjustable delay. The double column periphery is notified immediately through a fast hard-wired column OR. The pixel becomes insensitive and waits for a column readout token. When the token arrives the analog signal is sent to the periphery together with the pixel row address. For 160 pixels at least 8 bits are necessary. Because of technical reasons the pixel address consists of 9-bits (3×3 bits). The token is then passed on and the pixel resumes data taking. Thus, dead-time is short but depends on the hit rate of the DCOL.

In total each PUC contains 251 transistors.

4.1.2 Double Column Periphery

The double column periphery controls the transfer of hit information from the pixels to the storage buffers - called column drain mechanism. In addition DCOL periphery performs trigger verification. A schematic view of the logic is shown in Figure 4.3. When the asynchronous fast column OR signal arrives at the periphery three actions are performed:

- The present 8-bit value of the bunch crossing counter (WBC) is latched into one of 12 time stamp buffer cells. Storing the time stamp has to happen in less than 25 ns to allocate the hits to the appropriate bunch crossing. The time stamp is needed later on for trigger validation.
- The hits for this bunch crossing are acknowledged by the periphery. This signal notifies the pixels to associate any later hits with another column drain and its corresponding bunch crossing. There are one active and up to two pending column drains allowed. Hits of any further bunch crossings are lost.
- A column drain is initiated by sending out a readout token to the first pixel.

A pixel without a hit belonging to the active column drain just bypasses the token. This has been measured to happen at a rate of about 3.3 GHz analogous to 0.3 ns per pixel. That means the token arrives at the first hit pixel within less than 50 ns corresponding to 2 clock cycles. Hit information is transfered in parallel to the data buffer. Per pixel 2 clock cycles are needed. In total the time for a column scan to finish is less than 50 ns + (50 ns $\times$ number of hits). The average number of hits per DCOL is at high luminosity about 2.2 for the 4 cm layer. Therefore the column drain needs in average about 7 cycles. The data buffer has a depth of 32 units. Each unit consists of a marker bit, one analog and nine digital storage cells. The analog storage cell is for the pulse height and the digital cells are for the pixel row address. The marker bit indicates the beginning of a new event. It is used to synchronize entries in the time stamp and the data buffers. The oldest entry in the time stamp buffer is permanently compared to a Second Bunch crossing Counter (SBC). It is delayed with respect to the WBC by a programmable number of clock cycles which corresponds to the Level-1 Trigger latency. In case of agreement the time stamp is deleted and the presence of the CMS L1T signal is checked. Either the corresponding data is discarded or the DCOL is set into readout mode. In this mode, the DCOL stops data acquisition in order to prevent overwriting of valid data. It waits for the readout token to arrive and sends data to the chip periphery. Afterward the DCOL resets itself and hence cannot have further valid hits for the duration of the trigger latency. Data loss also occurs when one of the buffers is completely filled up. In case of a full data buffer the DCOL is reseted. If the time stamp buffer is full, data acquisition is paused until the next buffer cell is freed (Sect. 7.3).

4.1.3 Global Part

The global part of the ROC contains various control and supply circuits. It contains

- a serial programming interface. This is an I^2C-like protocol [28], modified to run at a speed of 40 MHz. To accommodate this high speed the possibility to read back configuration data had to be given up. Nevertheless, there is a limited read back possibility through the analog data stream which will be shown below. Two Low Voltage Differential Signal (LVDS) pairs are needed for clock and data lines.
- a fast signal decoder. First level triggers and commands for reset and calibration signal injection are coded into a LVDS signal (Sect. 3.4). This signal has to be decoded and distributed over the entire chip.

- 21 8-bit Digital-Analog Converters (DACs), five 4-bit DACs and one 3-bit DAC. The DACs are needed to adjust offsets, gains, thresholds, supply voltages, timings, etc.
- 2 control registers to set the trigger latency, readout speed (40 MHz/20 MHz) and the range for the calibration pulses. One bit is used to enable/disable the ROC.
- a band gap voltage reference and 6 voltage regulators. Three of them can be wire-bonded to external filter capacitors. This leads to a good immunity against power ripple and reduces chip-to-chip crosstalk. The ROC needs two external power supplies. 1.5 V for the analog section and 2.5 V for the digital part. It consumes a total of about 120 mW which corresponds to only 29 µW per pixel. The voltage regulators are programmable and hence the voltages can be set for each chip separately.
- an analog event generator. This is a circuit that collects the pixel hit information from the double columns and generates the output data stream as described in the next paragraph.
- an on-chip temperature sensor for monitoring cooling performance.
- a cluster multiplicity counter. This is a fast trigger signal that could be used by the CMS first level trigger or for self-triggering in the laboratory when no external trigger is available. Two thresholds can be set for this mechanism: one sets the minimal number of hits within a double column below which hits are considered as background and are ignored. The other one tunes the number of hit DCOLs above which a trigger signal is issued. Even below this threshold a signal proportional to the number of clusters is available.

In Reference [69] an exact description of the different pads, spy pads, the meaning of several DACs and the programming including the timing of the signals for operation can be found.

4.1.4 Analog Readout

The DCOL is insensitive between the time a trigger was validated and the time it finishes its readout. Therefore it is crucial with respect to data losses to minimize this readout time. The analog readout runs at 40 MHz (alternatively it can be switched to 20 MHz) and the pixel addresses are coded into 6 discrete levels. Each 3-bit group of the 9-bit pixel row address is converted by a 3-bit DAC to an analog level. Out of 8 discrete levels just 6 are used. The same principle is used for the DCOL address encoding. This permits to transfer the pixel address and signal pulse height in 6 clock cycles (Fig. 4.4).

The ROCs of a module are read out in a daisy chained way. The token bit, controlled by the Token Bit Manager chip, is sent to the first ROC. The ROC sends its data from the corresponding trigger to the TBM and passes the token bit to the next ROC. The TBM amplifies the analog signals and adds a header and a trailer to the data stream. The readout of a single pixel hit is shown in Figure 4.4. It starts with a header of 3 clock cycles. A large negative signal level well outside of the range of pixel data (ultra-black) followed by a zero differential level (black) separates the individual ROCs in the module data stream. No other identification is sent. In order to get the ROC identification the DAQ unit has to count the

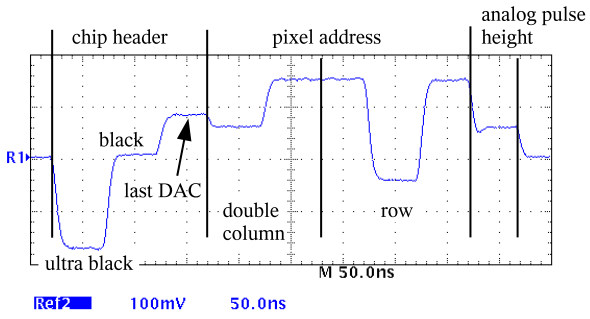

Figure 4.4: Readout sequence of readout chip with one pixel hit.

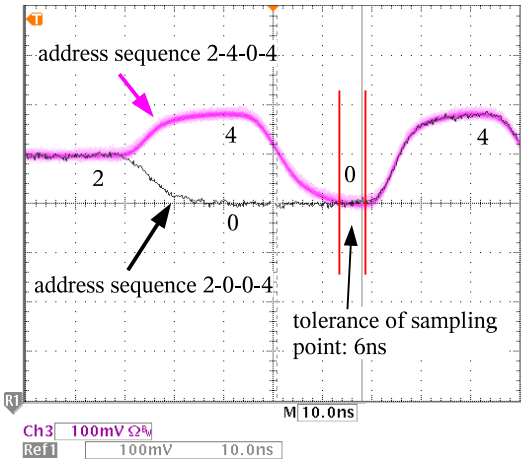

Figure 4.5: Readout signal output of a barrel module for two different address sequences and the sampling tolerance.

chip headers. In the third clock cycle of the chip header a signal inversely proportional to the value of the last addressed DAC is sent. This is the only way information about the configuration of the ROCs can be read back. It follows the double column address (2 cycles), the row address (3 cycles) and the analog pulse height for each hit pixel. Figure 4.5 shows the signal output of a barrel module as it arrives at the Analog Optical Hybrid (AOH). Shown are two different address level sequences. The rise-time of the signals is short enough to allow for a tolerance of the sampling point in the DAQ unit of about 6 ns. The measured level distribution for a ROC is shown in Figure 4.7. The address levels are clearly separated and allow a reliable reconstruction of the pixel addresses. Figure. 4.6 shows an eye diagram of the analog output signal at 40 MHz. It is a superposition of all possible pixel addresses which are analog coded in 6 discrete levels. Since the ROC has 26 DCOLs with 160 pixels each, the highest levels of the most significant bits are not used in the DCOL address and the pixel address. For more details concerning the PSI46V2 see Reference [70].

4.2 Radiation Damage Aspects of the Analog Chain of the ROC

The pixel detector is the innermost tracking device of the CMS detector. Therefore it has to survive in a harsh radiation environment. The radiation dose will be about 100 kGy per year during high luminosity operation which corresponds to about 6×10^{14} n_{eq}/cm^2. The detector has to work up to this fluence without any unacceptable degradation of its performance. With ongoing irradiation there will be a gradually change in the characteristic of the readout chip and the sensor. A consequence of this deterioration of performance is, that the lifetime of the ROC and the sensor is below the expected lifetime of the experiment. Hence the innermost layer of the barrel will have to be replaced after one year of LHC operation at high luminosity. In the next paragraphs the focus is on effects on the analog chain of the PUC due to ongoing

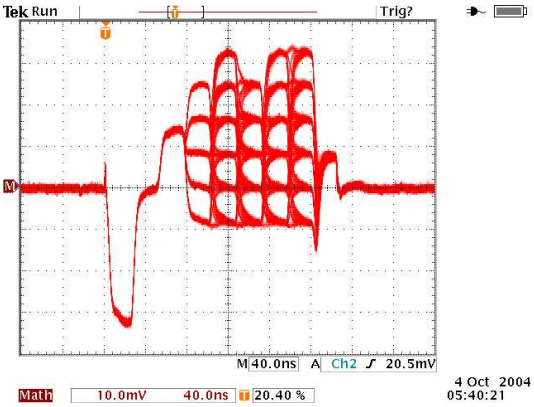

Figure 4.6: Eye diagram of the analog readout signal at 40 MHz. It is a superposition of readouts for all pixels of the ROC.

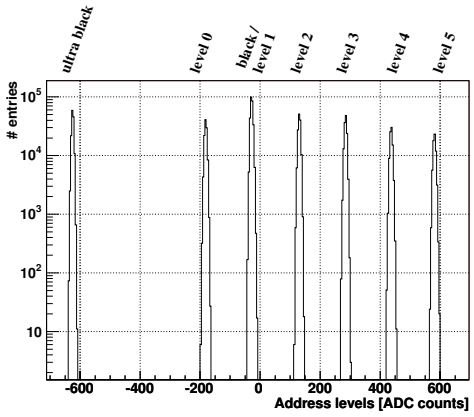

Figure 4.7: Histogram of the sampled address levels of a ROC. The levels are cleanly separated.

irradiation. The preamplifier has to deal with an increasing leakage current of the sensor and the performance of the amplifier is changing. The measurements were performed with PSI44 test structures. These test structures contain the same analog circuit like the pixel unit cell of the final ROC PSI46.

4.2.1 Sensor Leakage Current Tolerance of the Preamplifier

The increase of the leakage current I arises mainly from bulk generation centers introduced by the Non Ionizing Energy Loss (NIEL). The crystal defects add defect levels in the band gap. The exact effects of these levels depend on the energetic position in the band gap, but all of them will generate leakage currents. Accordingly, the change ΔI at total depletion is normalized to the sensitive volume V of the device. The variation of current with fluence Φ is expressed in terms of the damage rate α by

$$\frac{\Delta I}{V}(\Phi, T_A, t) = \alpha(T_A, t)\Phi. \tag{4.1}$$

ΔI denotes the current increase measured at a certain reference temperature T_R (mostly chosen to be 20 ℃) after an annealing time t at annealing temperature T_A (Sect. 3.2). For more details about the leakage current in irradiated silicon detectors see Reference [71].

The analog block of the PUC must be able to deal with the increased leakage current, since the sensor is DC coupled to the input pad. For an unirradiated sensor the accepted leakage current per module sensor is maximal 2 µA. Hence the leakage current per sensor pixel is about 30 pA which is negligible. Leakage currents of up to 50 nA are expected during the lifetime of the sensor and must be absorbed respectively driven by the preamplifiers. Due to the limited analog supply voltage of the amplifier, it will run into saturation if the leakage current is to high. The leakage current capability of the preamplifier was measured with the test structure PSI44 (Fig. 4.8). For the measurement the input pad was contacted with a high-resistance probe which was connected to a adjustable DC voltage source. By changing the output voltage the current was adjusted which mimics the leakage current. At the same

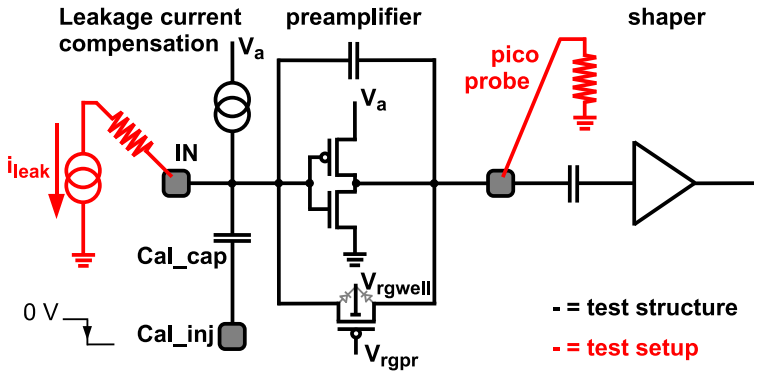

Figure 4.8: Schematic overview of the leakage current measurement.

time a test signal charge was given onto the amplifier input by the calibration-inject capacitor. For various leakage currents the output voltage of the preamplifier was measured. The output was accessible in the test structure by a spy pad. Figure 4.9 shows the signal pulse height at the preamplifier output as a function of the imposed leakage current from -500 nA to 50 nA for a V_{rgwell} voltage of 900 mV. V_{rgwell} is the potential of the nwell of the feedback pFET. No resulting output voltage was measured for positive leakage currents from the sensor. In this case the current is automatically absorbed by a p-n junction which is operated in forward direction in the feedback loop. The p-n junction is represented by the p implant of the pFET feedback transistor and its nwell. The curve shows that the analog block can provide at least 4 times the expected leakage current after one year operation at high luminosity. In addition to the measurement the result of the simulation for $V_{rgwell} = 900$ mV is shown which confirms the measurement.

According to the equation $U_a = U_i/R_i \times R_{fb} \Leftrightarrow U_a = I_{leak} \times R_{fb}$ one expects, that the preamplifier saturates at larger leakage currents for a smaller R_{fb}. Since the feedback resistor is represented by a pFET, the resistive path can be controlled by the nwell potential. Higher nwell potential means lower ΔU_{GS} and therefore a higher resistor. In Figure 4.10 the preamplifier output voltage versus the leakage current for various V_{rgwell} is plotted. That means the leakage current capability can be influenced by the settings of the preamplifier. The sensor pixels which are connected with a PUC at the edge or at the corner of the ROC have the double or fourfold area (Sect. 3.1.5). Since the leakage current scales with the volume these PUCs must be able to tolerate at least the fourfold leakage currents. This requirement could be already marginal. To increase the leakage current capability a programmable current source for compensation was implemented in each PUC in the PSI46. The current source is connected to the input node of the preamplifier and provides the leakage current if necessary.

4.2.2 Compensation for the Radiation Effects of the Analog Chain

The most sensitive part of a MOSFET to radiation is the SiO_2 gate oxide. By applying a voltage to the gate contact which is connected with the insulating SiO_2 layer, the conductivity of the MOSFET can be controlled. Regarding a nFET a positive gate-source voltage decreases the resistivity of the drain-source channel and vice versa.

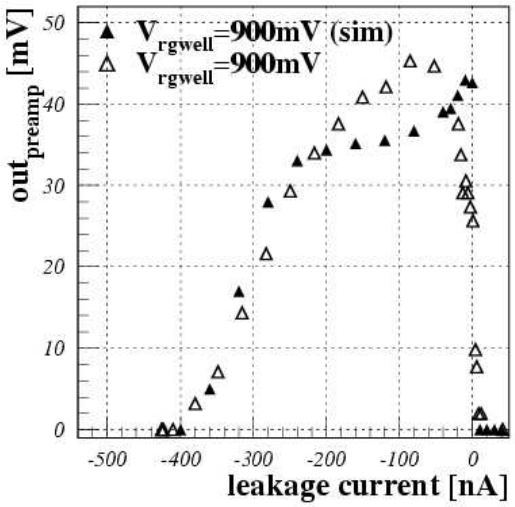

Figure 4.9: Output signal of the preamplifier for different leakage currents for V_{rgwell} of 900 mV.

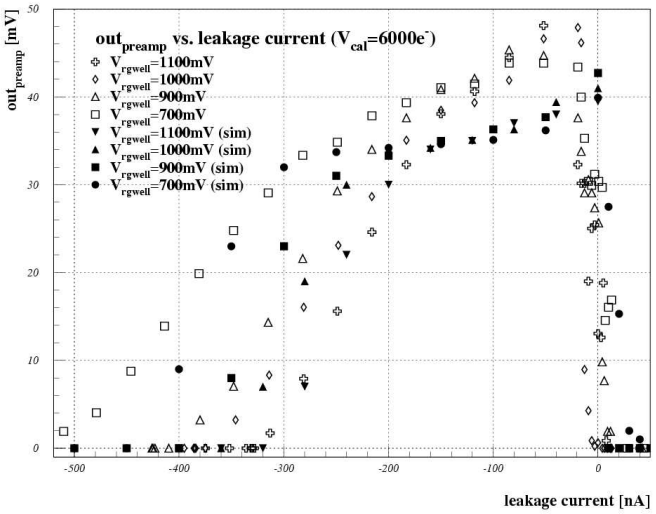

Figure 4.10: Output signal of the preamplifier for different leakage currents and for different V_{rgwell}.

The incoming ionizing radiation generates electron-hole pairs in the SiO_2 and in the substrate. These pairs quickly recombine and disappear partly. In the isolating gate oxide the electrons and holes behave differently as their mobilities are different. Immediately after irradiation, electrons will rapidly drift toward the positive gate electrode and holes will drift toward the Si/SiO_2 interface. At the Si/SiO_2 interface some fraction of the holes will be trapped by the crystal defects and form a positive oxide-trap charge. This causes an electron accumulation from the substrate close to the Si/SiO_2 interface in case of positive gate bias. Consequently the threshold voltage can change when the device is irradiated. The electron accumulation creates a negative threshold shift. In general the effect of radiation on the threshold voltage depends on the thickness of the oxide layer and therefore of the production process. Other consequences of the irradiation concern the gain and the shaping time of the circuit. In addition the oxide-trap charge causes in combination with the electron accumulation an increase of the leakage current from the drain to the source region of the nFET. Both, the leakage current and the threshold shift changes the electrical characteristics of the circuit. For more information see Reference [47].

The effect of the irradiation was investigated with PSI44 test structures. They have been irradiated up to 132 kGy with a ^{60}Co gamma source at PSI. Figure 4.11 shows the output signal of the shaper and the analog pulse height signal caused by a test charge injected at the calibration capacitor ("cal_cap" in Fig. 4.8). Contrary to the ROC, on the test structure the analog pulse height follows all the time the shaper signal. The red curves were measured before irradiation, the black ones after radiation and the green after readjusting V_{rgwell} of the feedback pFET for the preamplifier. The measurement shows that by readjusting the settings the electrical effects of irradiation can be compensated. The main effects of irradiation were an increase in gain and fall time. No degradation of the functionality was observed. The results agree with investigations of the RD49 collaboration [72].

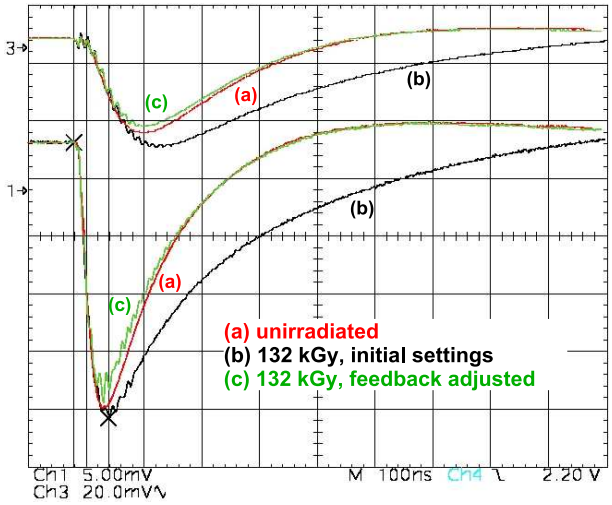

Figure 4.11: Output signal of the shaper (bottom) and the analog pulse height signal (top). The red curves (a) are before irradiation, the black ones (b) after irradiation and the green ones (c) with readjusted V_{rgwell} for the feedback pFET of the preamplifier.

4.3 Summary

At the Large Hadron Collider (LHC) every bunch crossing about 1000 charged tracks will emerge from the interaction point of the Compact Muon Solenoid (CMS) experiment. This results in a track density of 40 MHz/cm^2 at high luminosity for the innermost layer of the pixel detector. The CMS Level-1 Trigger (L1T) rate will be up to 100 kHz and the latency for the trigger decision is 3.2 µs.

Since the interesting events are quite rare the Readout Chip (ROC) must be able to run under LHC conditions in a mode of continuous data taking and simultaneous readout operation to keep the dead-time and the inefficiency as low as possible. To improve the accuracy of hit reconstruction by signal interpolation the analog pulse height is required. During the L1T latency the ROC has to register the pixel addresses and bunch crossing numbers of the hits. Because of the large number of pixels zero suppression is performed. To survive the harsh radiation environment of about 100 kGy/year for the innermost layer, a radiation tolerant design is required.

The ROC designed to fulfill these requirements consists of three major blocks with different functionalities: the sensitive pixel array organized in Double Columns (DCOLs), the DCOL periphery and a global part. The Pixel Unit Cell (PUC) contains a comparator in the analog part for zero suppression and 4 trim bits for a fine adjustment of the global threshold of the ROC. The pixel waits for hits and notifies the DCOL periphery to set the time stamps. The DCOL collects the data from the pixels and buffers it during the latency of the CMS trigger until the event is triggered or not. Not confirmed hits are discarded in the ROC. The triggered hits are read out after a token enters the ROC. In the global part of the ROC a programming interface, an event generator and 27 Digital Analog Converters (DACs) are implemented.

The ROC is fabricated in a commercial CMOS process which can be designed radiation

tolerant. It offers a smallest feature size of 0.25 µm and five metal layers for routing. Compared to the former used DMILL technology it is faster, has a lower power consumption and is cheaper.

The final ROC PSI46V2 has a physical size of 7.9 mm × 9.8 mm. The pixel array consists of 4160 pixels (100 µm × 150 µm in $r\phi \times z$) arranged in 52 columns and 80 rows. In total the PSI46V2 readout chip integrates about 1.3 million transistors and consumes about 120 mW.

The performance of the ROC was investigated up to a dose of 130 kGy. No degradation of the functionality was observed. The measured effects with ongoing radiation concerning the gain and the speed could be compensated by readjusting some internal DAC settings. In addition it was shown that the leakage current tolerance of the analog part of the pixel is sufficient to handle the expected leakage current of the sensor after 6×10^{14} n_{eq}/cm^2. To increase the leakage current margin a programmable leakage current compensation is implemented in each PUC in the final ROC design.

Chapter 5

Single Event Effects in the Readout Chip

A consequence of the high track density in the region of the pixel detector is the ongoing degradation of the performance of the readout chip and the sensor (Sect. 4.2). In addition to these gradual effects, there are Single Event Effects (SEEs). SEEs are caused when highly energetic particles present in natural space environment or in high energy physics experiments hit sensitive regions of microelectronic circuits. The traversing particle may cause no observable effect. On the other hand a transient disruption of circuit operation, a change of logic state, or even permanent damage to the integrated circuit may happen. The first predictions of SEE date back to 1962 [73] and have been confirmed in 1975 when upsets due to cosmic rays in certain space satellites were reported [74]. Today, SEEs are a well known problem and have been a continuous concern in space, aviation, and high energy physics [75]. There is a wide variety of effects produced by radiation. SEEs are characterized by a sensitive node, a threshold energy and a cross section. They result from charge deposition in a sensitive volume which is subsequent collected in a sensitive node. Each device is sensitive to SEEs only if a sufficient amount of charge is collected from the particle hit in the sensitive node. The minimum amount of charge is called critical charge Q_C. The cross section σ is the probability for a SEE to occur in a memory cell. It is measured as the number of events caused per unit fluence of particles and has therefore the unit cm^2/(memory cell). The importance of SEE considerations has increased for the experiments at LHC. It is especially for the pixel detector of CMS an issue since the probability for a SEE is proportional to the particle fluence. The expected fluence is about 2×10^{15} n_{eq}/cm^2 over the first ten years of operation. The intense hadron flux is according to simulations mostly composed of charged hadrons like pions and protons [76]. At the outer periphery the charged hadron flux is significantly reduced and neutrons emitted from the surrounding $PbWO_4$ electromagnetic calorimeter dominate. The focus in this Chapter will be on the investigations of Single Event Upsets in the readout chip of the pixel detector.

5.1 Single Event Upset

Single Event Upsets (SEUs) are so called "soft" SEE, since it is non permanent, i.e. their effects are reversible and correctable. A SEU is an instantaneous reversal of the logic state of an elementary memory register cell. The charge deposited by the incident particle in a sensitive volume and afterward collected in a sensitive node changes the state of the cell. Thus the original stored information is corrupted. An incident particle can also corrupt several bits at the same time. This phenomenon is known as Multiple Bit Upset (MBU).

The final ROC of the pixel detector is produced in the 0.25 µm technology, which offers a smaller feature size and a lower supply voltage compared with former processes like DMILL [20] (Sect. 4.1). A consequence of the smaller structures are the smaller node capacities e.g. of the gate contact of an inverter (Fig. 5.2). Considering the equation $U = Q/C$ the induced charge causes a higher voltage on the smaller capacitance. This effect is even intensified by the lower supply voltage, which reduces the threshold of e.g. an inverter. In addition, the quarter micron technology is faster due to the smaller capacities. Hence transients of at least 300 ps length can switch an inverter which is confirmed immediately by the second inverter in a standard memory cell consisting of 2 cross-coupled inverters. Consequently the probability for SEUs increases with the down scaling of the technology. In Reference [77] results of simulations and measurements for Q_C of different technologies are shown. Q_C is for a 0.30 µm technology with a supply voltage of 3.3 V about 20 fC (0.45 MeV) which corresponds to 125 ke$^-$. For the ROC in 0.25 µm technology with a digital operating voltage of 2.5 V the Q_C is expected to be even smaller. The critical charge depends not only on the technology but also on the memory cell design. The ROC has 4160 Pixel Unit Cells (PUCs) each containing 5 memory cells basically composed of two inverters. In the case of the ROC the memory cells are designed as Static Random Access Memories (SRAMs). 4 memory cells in a PUC are used for storing the trim bits. The fifth SRAM cell is used for enabling and disabling a pixel. Changing the fine adjustment of the global ROC threshold by switching the trim bits could be a serious problem, since the analog pulse-height information used for signal interpolation could be lost partly. For this reason the spatial resolution and the impact parameter resolution would get worse (eq. 2.12). But enabling a disabled noisy pixel is even more crucial for a entire DCOL since the time stamp buffers and data buffers will be flushed with entries. As a consequence the DCOL will be reseted all the time including the loss of all hits in the buffers (Sect. 4.1.2). The worst case is the switching of a memory cell in the global part of the ROC. Because all global DACs including their memory cells housed there. E.g. a change of the global threshold or supply voltage could make the entire ROC insensitive for hits. Consequently the SEUs are a potential danger to loose some vital detector control functions. It will not be a problem if only a small fraction of the data stream is corrupted by SEUs.

SEUs can be corrected by rewriting the information lost to the memory cell. Therefore error detection and correction techniques are crucial for handling SEUs. But the reprogramming causes data traffic and is restricted due to the limited number of digital optical links (Sect. 2.4.3) available for data transfer from the electronics room to the detector. The passage of an ionizing particle through a semiconductor device leads to the generation of electrons and holes in the target material. The subsequent collection of this charge in a sensitive node of the microcircuit is the fundamental mechanism causing SEUs. There are two methods by

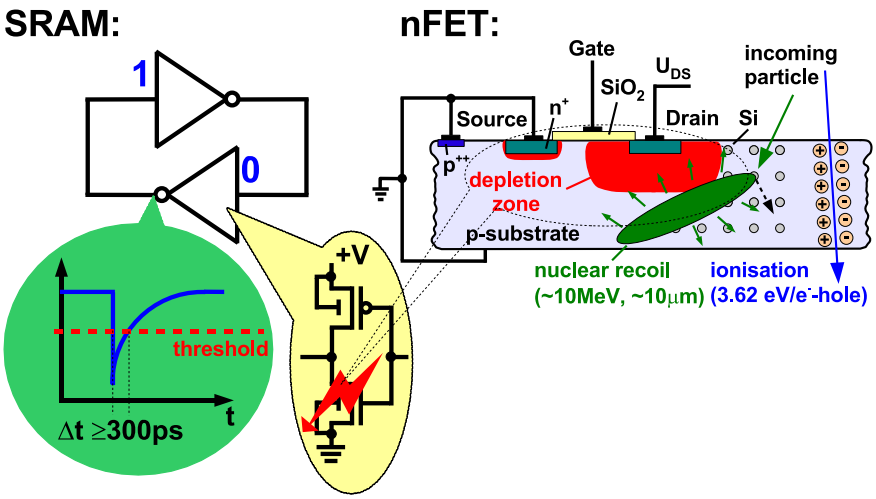

Figure 5.1: The right part shows charge deposition by direct and indirect ionization. The latter is used for particle detection. The former could cause a SEU if enough charge is collected in a sensitive node by diffusion and drift processes. The most sensitive region is the reverse biased p-n junction close to the drain contact. The induced charge can cause instantaneous reversal of the logic state of the SRAM cell.

which ionizing particles release charge in a semiconductor: direct ionization by the incident particle itself and ionization by secondary particles created by nuclear reactions between the incident particles and the struck device. Both can induce a SEU.

Direct ionization occurs when an energetic charged particle passes through a semiconductor material generating electron-hole pairs along its path as it loses energy (Fig. 5.1). The direct ionization is a coulomb interaction of the incident particle with the electrons of the target atoms. It is used for "regular" charged particle detection in the sensor. The deposited charge is in the range of a Minimal Ionizing Particle (MIP) (Sect. 3.2.1). For the pixel detector silicon sensor with a thickness of 285 µm, one MIP is about 23 ke^- (3.7 fC) which corresponds to a $dE'/dx' = 2.9$ MeV/cm. The deposited charge in the material is related to the Linear Energy Transfer (LET). The LET depends on the type and energy of the incident particles as well as the absorbing material. It is expressed by

$$LET = \frac{1}{\rho}\frac{dE'}{dx'}$$

ρ is the density in g/cm^3 and dE'/dx' is the mean energy transfered to the material per unit length path. Thus the unit of LET is MeV cm^{2}g^{-1} and is also referred to as stopping power. The LET can be seen as the energy loss per unit path length normalized by the density of the target material and is roughly independent of the target ($dE'/dx' = dE/dx \times \rho$ in Sect. 3.2.1). Direct ionization is the primary charge deposition mechanism for upsets caused by heavy ions. Usually lighter particles (e.g. protons) do not induce enough charge by direct ionization to cause upsets. Since devices become more susceptible, recent research has suggested that upsets in digital integrated circuits due to direct ionization by protons may occur [78, 79].

Although direct ionization by hadrons usually does not induce enough charge to cause upsets, protons, neutrons and pions can produce significant upset rates due to indirect ionization. As a high-energy hadron enters the semiconductor lattice may undergo a collision with a target nucleus and produce heavily ionizing nuclear fragments. Possible reactions are (Fig. 5.1):

- elastic collisions that produce Si recoils and lead to interstitials (atoms between regular lattice sites) and vacancies (empty lattice sites);
- the emission of alpha or gamma particles and the recoil of a daughter nucleus (e.g. Si emits a alpha-particle and a recoiling Mg nucleus);
- spallation reactions, in which the target nucleus is broken into two fragments (e.g. Si breaks into C and O), both can recoil;
- secondary processes from energetic displaced lattice atoms, respectively defect clusters from cascade processes.

Any of these reaction products can now initiate a full atomic cascade since each recoil can dislodge further atoms. All these reaction products deposit energy along their paths by direct ionization. According to Huhtinen and Faccio [76] the recoils typically have low energies about 10 MeV. Their range is limited to about 10 µm, which means that they have to be produced locally in the IC in order to cause a SEU. The tracks of the recoils terminate in the Bragg peak with a high energy deposition. Therefore they are called Highly Ionizing Particles (HIP) [80]. The recoils are heavy ions characterized by their charge Z. Their dE'/dx' scales at high energies roughly as Z^2. Thus the probability is low that a stopped proton can deposit enough energy and most probably heavy ions are responsible for causing SEUs. The dE'/dx' of a 10 MeV silicon recoil is about 30 GeV/cm - about 4 orders of magnitude above minimum ionizing. For details see [76, 77]. For a sensitive volume with a length of 1 µm the deposited energy is 3 MeV compared to 0.45 MeV necessary for switching of a memory cell in a 0.3 µm process.

The most sensitive regions for a SEU are reverse biased p-n junctions. Without an electrical field the semiconductor system goes back to thermal equilibrium by recombination of the electron-hole pairs after generation. The time for recombination is related to the charge carrier lifetime. The high external electrical field in the depletion region of a reverse biased junction is responsible for charge separation by drift processes. Therefore the charge is collected very fast ($\sim$nsec) and efficiently at the junction contacts where it causes a transient current. If the event occurs in the not depleted region but close to the vicinity of a p-n junction the charge is also collected by diffusion[1]. In this case the charge collection time is in the range of a few 10 nsec to 100 nsec in spite of the fact that some of the charge recombines before being collected.

The standard storage cell used in the ROC is composed of 2 cross-coupled inverters (Fig. 5.2). Different studies [81, 82, 83] have shown that for a given state of the memory cell, the two most sensitive points are the 2 OFF state transistors. More precisely the implant regions of the transistors (source or drain) where a reversed biased p-n junction occurs.

[1] An inhomogeneous distribution of free movable charge carriers result in diffusion.

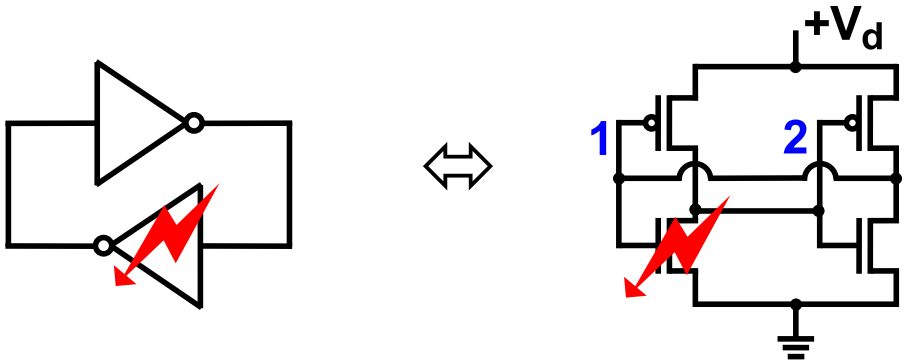

Figure 5.2: Schematic representation of a static memory cell composed of 2 cross-coupled inverters (the access transistors are not shown) The arrow indicates the charge deposition. 1 and 2 denominate *node_1* and *node_2*.

For the following example *node_1* is on *gnd* potential and *node_2* is on V_{dd} in the initial state of the storage cell (Fig. 5.2). The incident particle induces charge in the vicinity of the OFF nFET[2] (indicated by an arrow in Fig. 5.2). The electrons are collected to the capacitive load of the struck node, which is the drain of the nFET being on V_{dd} potential. The capacitor is mainly represented by the input node of the second inverter (*node_2*). If the collection process is fast enough and the collected charge is larger than the critical charge Q_C, the potential of the struck drain decreases the input threshold of the second inverter ($U_{initial\_node\_2} + \Delta U < U_{thr}$ with $\Delta U = Q_{collected}/C_{struck\_node}$). Therefore the second inverter switches and in turn reinforces the change of state at the output of the struck inverter. The result is the reversal of the logic state of the memory cell. The electrons collected at the drain of the nFET can be evacuated to V_{dd} through the pFET, which represents a resistive path (though the resistance is low, as the transistor is ON). Essential for the prevention of a SEU is that the discharging of the drain node is fast enough. The time constant for discharging is: $\tau_{discharge} = R_{ON\_pFET} \times C_{struck\_node}$. For switching the inverter, the potential at the input node has to be at least about 300 ps above or below the threshold [84]. To reduce the probability for a SEU one could decrease the time constant for discharging $\tau_{discharge}$ or lower ΔU resulting from the collected charge on the capacitive load of the sensitive node. The time constant is minimal since the transistor is switched on and it is operated in the linear region. The capacitive load is due to the use of minimal transistors also minimal. To reduce $\Delta U = Q_{collected}/C_{struck\_node}$ one has to increase the capacitive load of the output node of the inverter by adding a capacitor to *gnd* potential. Doing this results in two additional capacitors per memory cell (Fig. 5.3). The same benefit is gained with a single capacitor C_{ex} between the outputs of the inverters. In the case of the example *node_2*, which is on V_{dd}, decreases its potential due to the collected electrons. Therefore the potential at *node_1* is drawn below *gnd*. That means the second inverter has to discharge C_{ex} and subsequently charge it up to V_{dd}. This procedure needs more time than charging from *gnd* to V_{dd}. Since ΔU at the input

[2]The ROC is produced in a commercial 0.25 µm technology which is a Complementary Metal Oxide Semiconductor (CMOS) process. A simple inverter consists of a serial combination of a pFET and a nFET (Field Effect Transistor).

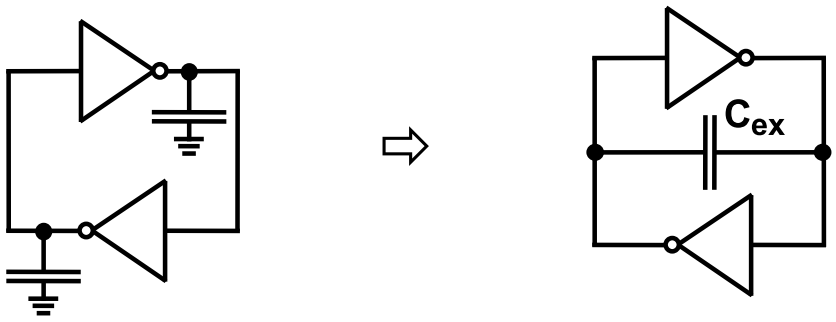

Figure 5.3: Left side: Protected static memory cell composed of 2 cross-coupled inverters each protected with a capacitor. Right side: Protected static memory cell protected with one capacitor.

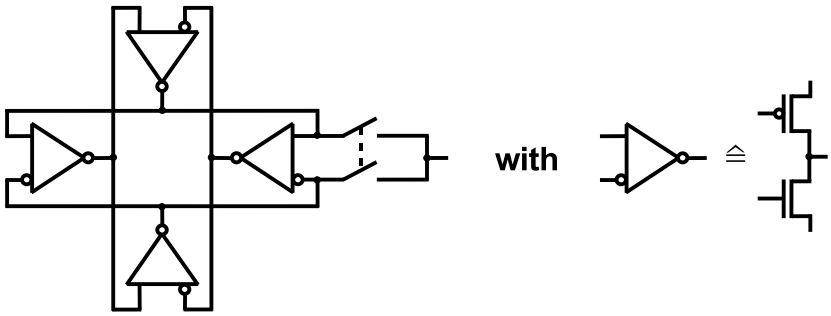

Figure 5.4: Schematic representation of a dual interlock storage cell. This memory cell needs simultaneous writing to two nodes for switching.

of the inverter is just a transient effect, the time is too short to charge C_{ex} up to the threshold voltage of the input of inverter 1. Thus the reversal of the logic state is suppressed. Because of the additional capacitance the minimal time required for programming the memory cells is increased. However, the programming time is in this case not a critical issue for the ROC.

Another approach to reduce the probability for SEUs is the Dual Interlock storage Cell (DICE) [85]. The DICE cell needs for switching the simultaneous writing to two separate nodes. These nodes can be placed in the design with spatial distance to ensure that a single incident particle can not simultaneously induce charge to both sensitive nodes. The basic schematic of this memory cell is shown in Figure 5.4. A different method to improve the SEU resistance is to triple every SRAM cell and read out always the three memory cells together with a majority building logic. A disadvantage of this approach is the increase of the number of transistors and the needed threefold area at least. Therefore this method was ruled out as possible solution for the ROC, since the space available in a PUC is limited.

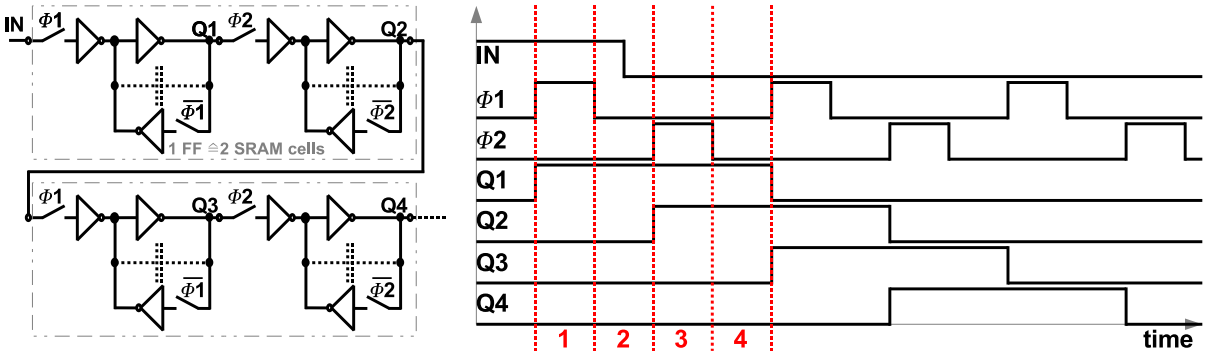

Figure 5.5: Two flip-flops of the shift register each consisting of two SRAM cells. The switches are integrated in the inverter structure. Each complete Φ1-Φ2 cycle consists of 4 clock cycles and shifts the stored bit by one flip-flop.

5.2 Test Structures

To investigate the SEU sensitivity of different memory cells simple test structures have been fabricated in DSM technology. To get more statistics, since SEUs are rare events, shift registers containing 500 Flip-Flops (FFs) in series have been designed. A flip-flop, also called bistable trigger circuit, is a clocked digital circuit capable of serving as a one-bit memory cell. It is composed of two consecutive SRAM cells which are set up in a linear fashion which have their inputs and outputs connected together in such a way that the data is shifted down the line when the circuit gets the corresponding clock signals (Fig. 5.5). The signals Φ1, Φ2 and IN in the following paragraph are indicated in Figure 5.5. The additional inverter beside the two cross-coupled ones of the SRAM cell ensures the operation of the storage cell and guaranty that all memory cells are loaded with the same logical state. The switches are integrated in the inverter structures (appendix A). The test structure contains three different shift registers each 500 FF cells long. The flip-flops of the different registers are composed of two:

i) standard SRAM cells designed of two cross-coupled inverters without any protection against SEUs (Fig. 5.5).

ii) standard SRAM cells designed of two cross-coupled inverters with an additional capacitor of $C_{ex} = 75$ fF connecting the outputs of each SRAM cells for protection (Fig. 5.5).

iii) DICE cells (Fig. 5.4).

The standard SRAM cells are the same like the ones used in the ROC. They have been lay outed as dense as possible to be sensitive for multiple bit upsets if necessary. The over-all meandering arrangement of the shift registers was identical for all three register types. For the operation of the shift registers a couple of additional inverters were necessary to generate the inverse clock phases and to drive 1000 SRAM cells in parallel with the clock signals. In total for the operation of the test structures the supply voltage and two clock signals Φ1 and Φ2 are necessary. For the access to the content of the shift registers an IN and OUT pad is available. The OUT signal is the output of FF 500 amplified by a line driver.

Due to a design error the shift register composed of DICE cells didn't work. The pFET or the nFET in the basic cell of the DICE cell must be always stronger for a proper functioning

(Fig. 5.4). This causes in the shift register composed of DICE cells a backward shifting of the logic state. To prevent this action inverters have to be implemented between the consecutive DICE cells of the shift register.

5.3 Beam Tests

The charged hadron flux in the region of the pixel detector consists mainly of pions and protons. The energy spectrum peaks in the range of about 200 MeV to 1 GeV [76]. The goal of the beam test was to determine the cross section for SEUs and to investigate the benefit of the protection capacitor in a comparison to an unprotected SRAM cell.

The beam test took place at the πE1 beamline at the Paul Scherrer Institut. The beamline was used with a beam momentum of about 300 MeV/c for the pions (π^+ and π^-) and with a momentum in the range of 500 MeV/c for the protons [86]. The pion fluence was determined by activation of Al foils with incident pions: ^{27}Al($\pi^{\pm}$,xN)^{24}Na. By measuring the resulting γ(1369 keV) decay activity of Na the pion fluence was determined with the well known cross section of the primary monitor reaction [87]. With a ionization chamber positioned at the outlet of the beam pipe a calibration factor was determined to find out the corresponding fluence for each measurement.

5.3.1 Pion Beam Test with Test Structures

Four test structures were exposed in parallel to pions (π^+) with a momentum of 300 MeV/c in September 2003. The appropriate pion flux through the Device Under Test (DUT) was about 1.3×10^9 cm^{-2}s^{-1}. The angle of the incident pion beam was perpendicular to the surface of the test structures. For the operation of the test setup a PC with a multi channel I/O card was used. The PC provided the test structures with Φ1,Φ2 and the IN signal. The 8 OUT signals of the shift registers were read by the I/O card too. For fluence determination the ionization chamber was also read out together with the test structures. The 8 separate shift registers, 4 without and 4 with additional capacitors, were loaded with a logical state (HIGH$\equiv$1 or LOW$\equiv$0). Before reading out the content of the test structures with the switched FF if so, the shift registers have been irradiated for 5 minutes. After this delay time, the shift registers were read out and loaded simultaneously by clocking the initial state into the registers. The output was stored to a data file. By counting offline the switched FF and calculating the fluence, the cross section for SEUs was determined. This procedure was repeated several times to get enough statistics for different supply voltages and different initial states. Since the test structures were produced in DSM technology, the supply voltages have been 1.5 V, 1.75 V, 2 V, 2.25 V and 2.5 V. With increasing supply voltage a decreasing SEU cross section was expected (Sect. 5.1).

5.3.2 Proton Beam Test with the Readout Chip PSI46V1

The second part of the beam test investigating SEU effects took place in December 2003. The SEU measurements were done in conjunction with a high rate beam test of the first version of the DSM ROC PSI46V1 assembled with a single-chip sensor. The submission of the PSI46V1

contained different ROCs with protected and unprotected storage cells. At this time the influence of the area of the so called MIM capacitors (Metal Insulator Metal capacitors)[3] on the yield was not clear. The setup for the operation of the PSI46V1 and the results from the beam test can be found in [65, 67]. During this test period for the SEU measurements 300 MeV/c $\pi^{\pm}$ and protons with a momentum of 500 MeV/c were used. The flux of π^+ (π^-) was 87.8 MHz/cm^2 (84.5 MHz/cm^2) and for the protons the flux was 151.2 MHz/cm^2. The ROC has in each PUC a memory cell which can be used to enable or disable the pixel cell (Sect. 4.1.1). A disabled pixel can not initiate a column drain. To be sensitive for SEUs, all pixels of the ROC have been disabled/enabled before exposure to the beam. Exposure times varied from 6-14 hours. After this period of time the number of SEUs was determined by giving test pulses to each pixel and counting the responding PUCs respectively the not responding PUCs.

5.4 Results and Discussion

In Figure 5.6 the measured cross sections versus the supply voltages for the test structures are shown. Exemplary in Figure 5.7 the summary histograms of the 8 shift registers, operated with 1.5 V, are plotted for the initially loaded state 0. The arrays of the unprotected (top) and with a capacitor protected shift registers (bottom) are presented after an total exposure time of nearly 13 h, which corresponds to about 160 measurements of 5 minutes. The results from the measurement with the PSI46V1 are shown at the corresponding internal digital voltage of 1.8 V, which is the operating voltage for the PUC storage cells. The results for the ROC measurement were achieved by counting the pixels which did not respond to the test pulses (Fig. 5.8). One of the most obvious results is the decreasing of the measured SEU cross sections for higher supply voltages. This was already discussed in Section 5.1 and shows a behavior as is expected. For clarification the further discussion of the results is based on the cross sections at 2 V for the test structures. For other supply voltages, the corresponding numbers can be calculated with the exact values in Table 5.1 and 5.2. $0\rightarrow1/1\rightarrow0$ indicates the switching direction. The first number is the initially loaded state. The "-" in some fields in Table 5.2 indicates that no measurement was performed. In this cases the cross sections for the most probable switching direction (unprotected SRAM cells) are already low. Therefore no SEU was expected in a reasonable time and the measurements for the protected SRAM cells or the suppressed switching direction for the unprotected cells have been omitted.

5.4.1 Protection Capacitor

For the test structures the benefit of the protection capacitor is in the range of 150/135 ($0\rightarrow1/1\rightarrow0$). In the case of the ROC the benefit is for π^+ ($0\rightarrow1$) about 94. For $1\rightarrow0$ the benefit is not serious since for the protected FFs no SEU has been found after 13 h and therefore 1 SEU was assumed to calculate the upper limit of σ. The different cross sections

[3]The MIM capacitors are formed by an additional thin layer of metal between metal layer 2 and 3 in the used 0.25 µm process. The total area of MIM capacitors is restricted by the design rules to 1 mm^2 per ASIC. In the ROC with the protection capacitors the total area is about 3.5 mm^2. Therefore it was not clear if the yield of the ROCs suffers from the area of the MIM capacitors.

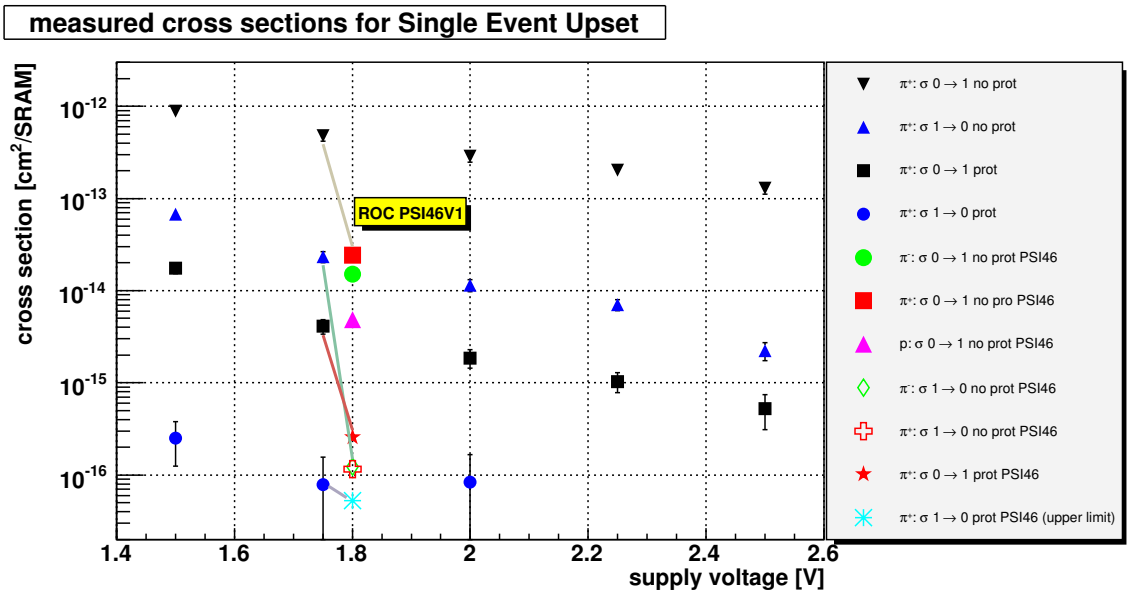

Figure 5.6: Single event upset cross sections for the protected and unprotected storage cells measured with the test structures and the ROC PSI46V1. The markers of comparable measurements of the ROC and the test structures are indicated by lines.

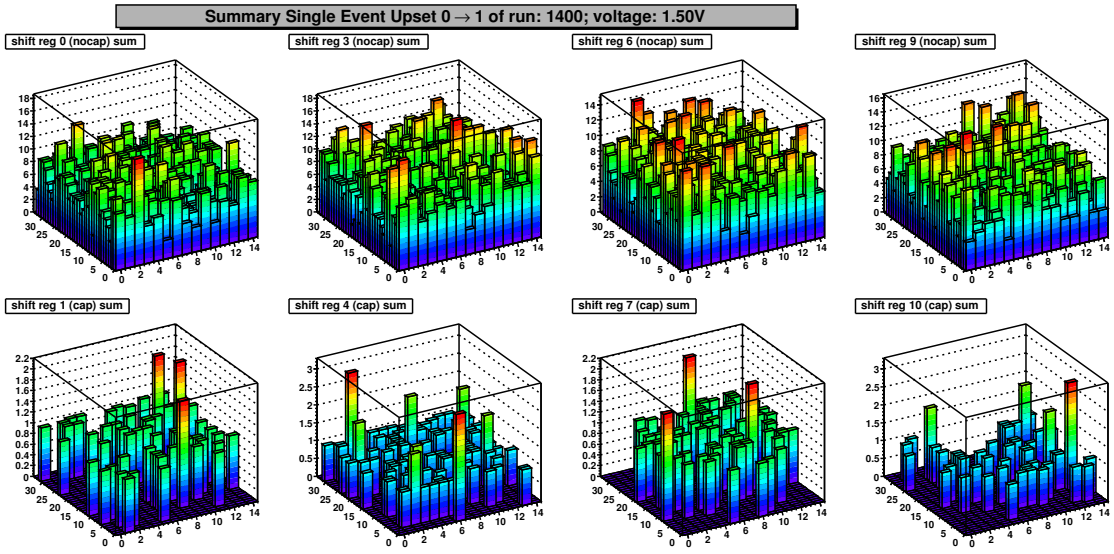

Figure 5.7: Summary histograms of 4 test structures operated in parallel at a supply voltage of 1.5 V after exposure of about 13 h to a pion (π^+) beam. The SEU distributions for unprotected (top) and protected SRAM cells, initially loaded with 0, are shown. The FFs are arranged in arrays of 15×34.

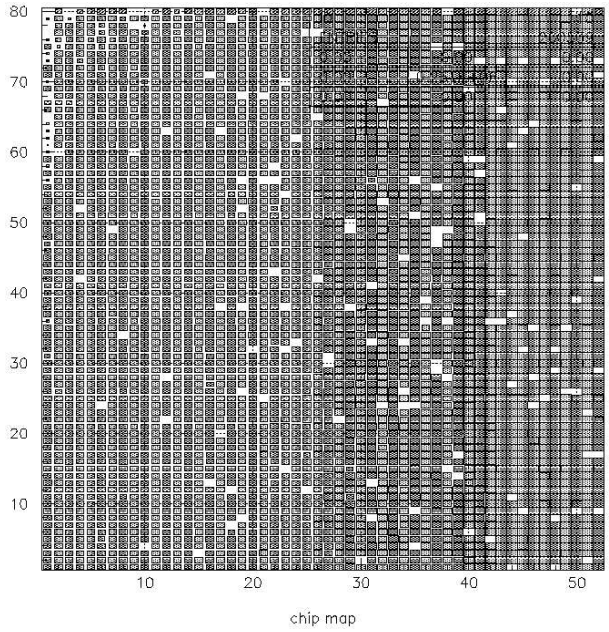

Figure 5.8: Readout chip PSI46V1 pixel map (52 columns $\times$ 80 rows) after 13.5 h exposure to a proton beam of 157 MHz/cm^2. The number of switched off pixels due to SEUs is 145. The pixel map was generated by injecting calibration pulses.

cross sections for test structures (π^+) in 10^{-14} cm^2/SRAM				
voltage (V)	unprotected		protected	
	0→1	1→0	0→1	1→0
1.5	88.9	6.74	1.76	0.0251
1.75	47.9	2.33	0.412	0.00784
2.0	28.7	1.15	0.186	0.00839
2.25	20.2	0.701	0.104	0.0061* [$\approx$ 15 h]
2.5	12.9	0.224	0.0526	0.0086* [$\approx$ 11 h]

Table 5.1: SEU cross sections for the test structures with protected and unprotected SRAM cells. The measurements were performed with a π^+ beam at various supply voltages. The shift registers have been initially loaded with 0 or 1 (* means upper limit [no SEU registered in # hours]).

cross sections for PSI46V1 in 10^{-14} cm^2/SRAM				
beam	unprotected		protected	
	0→1	1→0	0→1	1→0
π^+	2.42	0.0115	0.0257	0.00529* [$\approx$ 12 h]
π^-	1.51	0.0123	-	-
proton	0.486	-	-	-

Table 5.2: SEU cross sections measured with the readout chip PSI46V1 in a proton and a $\pi^\pm$ beam for both switching directions. The SRAM cells were operated with 1.8 V (* means upper limit [no SEU registered in # hours]; - means no measurement performed).

from the ROC and the test structure could be explained with slightly different layouts. E.g. the capacitive loads for the SRAM cells are not the same in PSI46V1 and the shift registers. This can cause the different resulting effects of the protection capacitors. Concerning the yield of PSI46V1 there was no difference seen for the two types (Sect. 5.3.2) of the ROC. The yield for the ROCs with and without MIM capacitors for SEU protection was better than 80 %. Therefore it was decided to use in the final ROC PSI46V2 the protected SRAM cells for the trim bits and the mask bit in each PUC. The registers of the global DACs are also protected with capacitors. Since writing to the data and time stamp buffers is more time critical during a running column drain, these memory cells are unprotected. Anyway a small fraction of corrupt data is acceptable.

5.4.2 Asymmetry in Switching Direction

For the shift registers the asymmetry related to the switching direction 0→1/1→0 is for the standard FFs approximately 25 compared to about 22 for the protected FFs. In the case of the ROC the asymmetry 0→1/1→0 is for π^- roughly 120 for the unprotected FFs. The measured asymmetry could be interpreted with the different mobilities of the holes and electrons in Si. According to Sze [88] the mobility for e^- is 1450 cm^2/Vs compared to 450 cm^2/Vs for holes. The consequence of the asymmetry is different for the five SRAM cells per PUC in the ROC. In the case of the mask bit, which is used to enable/disable the pixel, 0 means enabled and 1 means disabled. Therefore the 0→1 switching direction which disables the pixel is more probable. Loosing single pixels is only a minor operational problem. The more serious problem of enabling a noisy pixel is suppressed. Concerning the trim bits 0 means not trimmed and 1 means trimmed. Trimming lowers the threshold. This means that the more probable switching direction lowers the threshold and causes finally more DCOL resets and corresponding data loss (Sect. 5.1). Hence the asymmetry is in the case of the trim bits a disadvantage. The idea for the next ROC submission is to implement just one more inverter per trim bit to store the opposite logic state and benefit from the asymmetry. Applying this the consequences of a SEU could be reduced.

5.4.3 Comparison of p and π^-

Comparing the cross sections for the ROC of 500 MeV/c protons with 300 MeV/c π^+ (0→1) the impact of pions concerning SEUs is 4.7 times worse. According to Huhtinen [89] the measured pion/proton asymmetry is reasonable. To crosscheck this ratio one has to simulate the three dimensional charge deposition in the semiconductor caused by hadronic interactions with 300 MeV/c pions and 500 MeV/c protons [76]. Afterward one has to simulate the diffusion and drift effects to get the correct charge collection time structure at the sensitive node. This charge time structure is the input for a electrical circuit simulation to get the probability for switching a SRAM cell.

5.4.4 Multiple Bit Upset

For the investigation of multiple bit upsets the number of expected double SEUs was calculated and compared to the counted number of double SEUs. Since the shift registers have been lay outed in the form of arrays with 15 columns and 34 rows a double SEU was defined as a switched FF with a consecutive changed FF in the next row or column. Therefore 4 consecutive FFs are checked. The diagonal FFs were not taken into account. To have enough statistics exemplary a run at 1.5 V with 0→1 was chosen. The number of SEUs per readout of 500 FFs was fitted with a Poisson distribution. The *mean* was after a delay time of 5 min approximately 44 SEUs per readout at a flux of 1.3×10^9 cm^{-2}s^{-1} (Fig. 5.9). With this number one can calculate the expected number n_{exp} of double SEUs per readout with the equation[4]

$$n_{exp} = \sum_{n=1}^{mean-1} n \frac{n_x}{n_{tot} - n} \tag{5.1}$$

$n_x = 4$ is the number of consecutive FFs taken into account for double SEUs and $n_{tot} = 500$ is the total number of FFs per shift register. The expected number of double SEUs is then $n_{exp} = 8.0$. These 8 double SEUs are expected due to purely statistical reasons after 5 minutes. The comparison with the counted number of double SEUs is shown in Figure 5.10. The mean of the counted double SEUs is about 7.5 and in the range of the expected number of 8. A counted number of double SEUs significant higher than the expected number would have been a hint for correlated SEUs. To crosscheck this result the distances of changed FFs were histogrammed summed. For a random process an exponential distribution of the distances is expected. The result of the crosscheck is shown in Figure 5.11. No hint for correlated SEUs have been found. Especially in the case of the tilted test structures the investigation of the MBUs was interesting. The angle between the incident beam and the DUT was about 12°. Therefore the path length of a traversing particle close to a sensitive node is increased. Thus the probability for an SEU is higher compared to the perpendicular case. The extension of one FF in the shift registers is in the range of 38.7 µm × 18 µm. The beam particles may traverse more than one FF and the generation of a MBU is more probable. In Figure 5.13

[4]Equation 5.1 is derived by assuming one FF with a SEU. The probability for finding the next SEU consecutive to the first one is 4/499. Having already two SEUs the probability for the third SEU is 8/498 to be next to an former SEU and so on. Finally one has to sum up to the total number of expected SEUs. The number of expected SEUs is the *mean* of SEUs per measurement (Fig. 5.9).

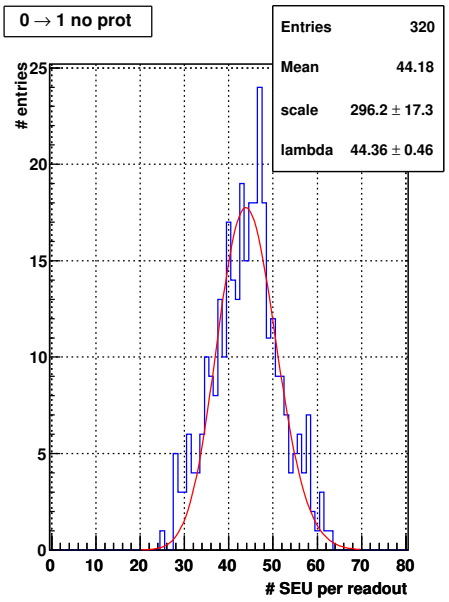

Figure 5.9: The number of SEUs per readout is histogrammed. The shift register without protection was operated with a supply voltage of 1.5 V and initially loaded with 0. The mean is 44 SEUs in 500 FFs after 5 minutes.

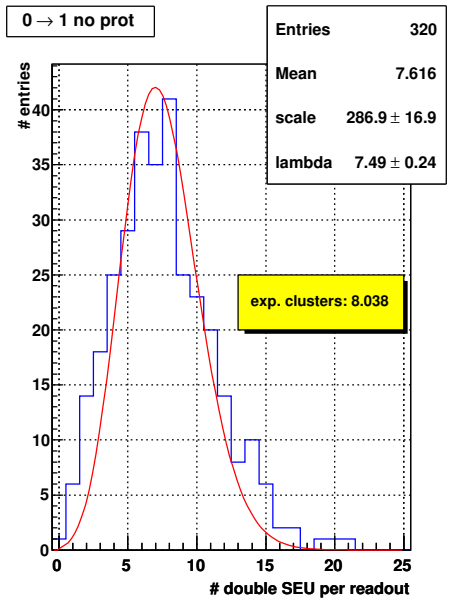

Figure 5.10: The number of double SEUs per readout is histogrammed. For 44 SEUs per readout (Fig. 5.9) the expected number of double SEUs is about 8 (exp. clusters). Counting the number of double SEUs gives on average 7.5 double SEUs.

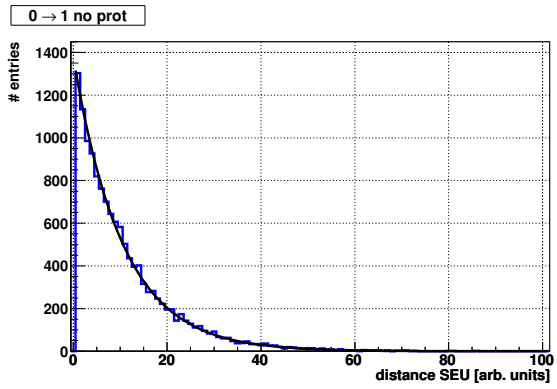

Figure 5.11: The distance of two consecutive SEUs is shown for the same run like in Fig. 5.9 and Fig. 5.10. For not correlated SEUs an exponential distribution is expected.

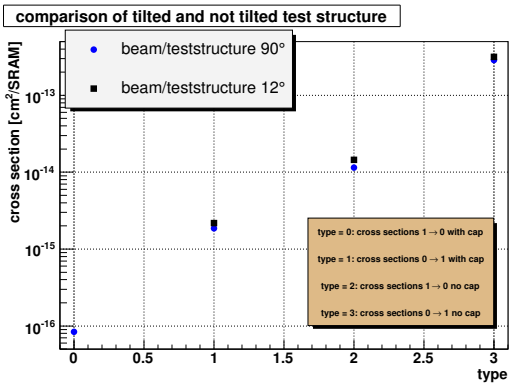

Figure 5.12: Cross sections for the tilted test structure compared to the not tilted test structure. The angle between the incident beam and the test structure was 12°.

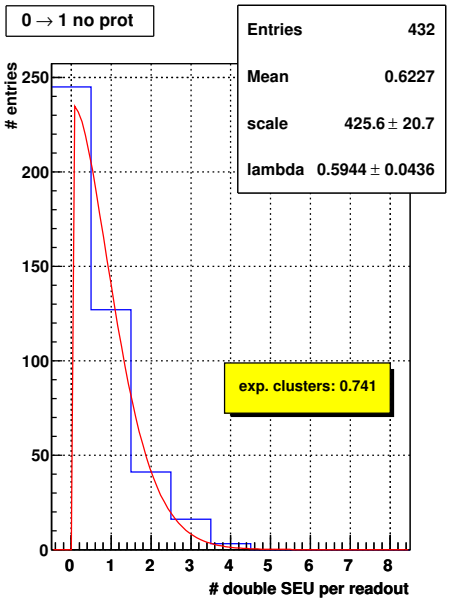

Figure 5.13: The number of double SEUs per readout for the tilted test structure is histogrammed. For 14 SEUs per readout the expected number of double SEUs is about 0.7 (exp. clusters). Counting the number of double SEUs gives on average 0.6 double SEUs.

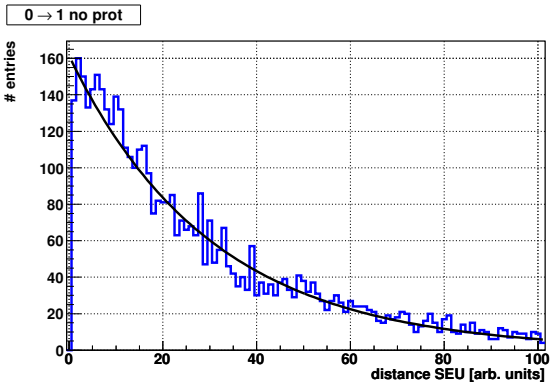

Figure 5.14: The distance of two consecutive SEUs is shown for the tilted test structure for the same run like in Fig. 5.13. For not correlated SEUs an exponential distribution is expected.

the number of double SEUs per readout for the tilted test structures is shown. The counted number of double SEUs of 0.6 corresponds to the expected number of 0.7. The distances of the SEUs are histogrammed in Figure 5.14. It shows an exponential decay and therefore even in the case of the tilted test structure no hint is given for MBUs.

5.4.5 Tilted Test Structure

The cross sections for a tilted test structure at a supply voltage of 2 V have been measured. The angle between the incident pion beam and the surface of the tested device was 12°. For both switching directions the protected and unprotected SRAM cells showed the same sensitivities for SEUs like the not tilted test structures (Fig. 5.12).

5.4.6 Comparison of π^+ and π^-

Concerning the ROC the ratio of the cross sections for π^+/π^- is for the unprotected SRAM cell 1.6 (0→1) and 0.97 for 1→0. Since Si is a symmetrical nucleus, no difference was expected for π^- and π^+ [90].

PSI46V1			SEUs/ROC/sec			SEUs/sec		
prot	π^+	$\sigma_{(cm^2/SRAM)}$	layer 1	layer 2	layer 3	layer 1	layer 2	layer 3
no	0→1	2.42×10^{-14}	2.01×10^{-2}	1.01×10^{-2}	4.03×10^{-3}	$4.64\times10^{+1}$	$3.87\times10^{+1}$	$2.16\times10^{+1}$
no	1→0	1.15×10^{-16}	9.57×10^{-5}	4.78×10^{-5}	1.91×10^{-5}	2.20×10^{-1}	1.84×10^{-1}	1.03×10^{-1}
yes	0→1	2.57×10^{-16}	2.14×10^{-4}	1.07×10^{-4}	4.28×10^{-5}	4.93×10^{-1}	4.11×10^{-1}	2.30×10^{-1}
yes	1→0	5.29×10^{-17}	4.40×10^{-5}	2.20×10^{-5}	8.80×10^{-6}	1.01×10^{-1}	8.45×10^{-2}	4.73×10^{-2}

PSI46V1		SEUs/link/sec		sec for 1‰ per link		tot SEUs/sec
prot	π^+	layer 1&2	layer 3	layer 1&2	layer 3	total barrel
no	0→1	$2.58\times10^{+0}$	7.73×10^{-1}	310 (≈**5 min**)	1033 (≈**17 min**)	**106.7**
no	1→0	1.22×10^{-2}	3.67×10^{-3}	65217 (≈**18 h**)	217391 (≈**60 h**)	**0.51**
yes	0→1	2.74×10^{-2}	8.21×10^{-3}	29183 (≈**8 h**)	97276 (≈**27 h**)	**1.13**
yes	1→0	5.63×10^{-3}	1.69×10^{-3}	141777 (≈**39 h**)	472590 (≈**131 h**)	**0.23**

Table 5.3: The calculated SEU rates for different layers, control links and the entire barrel of the pixel detector based on the measured SEU cross sections for the ROC PSI46V1 (prot. means with or without protection capacitor). The calculations were made for the following fluences corresponding to $\eta = 0$: 40 MHz/cm^2 (layer 1), 20 MHz/cm^2 (layer 2), 8 MHz/cm^2 (layer 3). The SEUs per second and per control link and the SEUs per second for the entire barrel are the crucial numbers since all pixel FECs are in the same VME crate.

5.4.7 Impact of Clock Level

The influence of the signal levels of $\Phi1$ and $\Phi2$ during the delay time on the cross section was investigated. No impact was seen.

5.4.8 Consequences for the Control System

After a memory cell gets corrupted by a SEU it can be corrected by rewriting the information lost to the storage cell. The reprogramming causes data traffic which is limited by the number of digital optical links transferring the data from the FEC to the front-ends. One digital optical link controls 12 modules (Sect. 2.4.3). Either 4 modules of the first layer in combination with 8 modules from the second layer or 12 modules of the third layer. The pixel FECs are located 100 m away from the detector in VME crates in the electronics room.

The consequences of the measured SEU cross sections for the control scheme can be seen in Table 5.3. The expected SEU rates are based on the SEU cross sections measured with PSI46V1. The reprogramming of the SRAM cells in 1 pixel needs about 40 clock cycles corresponding to 1 µs. The pixel detector control system is designed in such a way that reloading the settings without stopping data taking is possible. The convenient time for such operations would be the LHC abort gap (3.2 µs) every 88 µs or the CMS "private orbits" (88 µs without triggers). In both periods just a few pixels of the 48×10^6 pixels could be reprogrammed. An additional problem would be the algorithm which monitors very efficiently the noisy and dead pixels to select in a sophisticated way the pixels having to be reloaded. Alternatively a kind of "simple" reloading could be preformed which means that a certain amount of pixels are reprogrammed in every gap without any selective approach. In spite of

these methods a certain percentage of memory cells would be in always corrupt. Therefore the SEU issue has been considered always as a serious problem in the past. For the DMILL ROC the SEU cross section was in the range of 2.4×10^{-13} cm^2/SRAM [91] compared to 2.57×10^{-16} cm^2/SRAM for the DSM ROC. This is about 3 orders higher. This means for the optical links, which control the first and second layer that in half a minute 1‰ of all SRAM cells are concerned by a SEU. In the case of the DSM ROC the corresponding time is about 8 hours (Table. 5.3). This results in about 1 SEU per second for the entire pixel detector barrel (48×10^6 pixels). According to the cross sections measured with the PSI46 with protected SRAM cells the expected SEU rates per control link are sufficiently small. Hence most likely reloading single pixel cells during data taking can be avoided [21].

5.5 Summary

A Single Event Upset (SEU) is an instantaneous reversal of the logic state of a memory cell, caused by a high energy deposition in a small sensitive volume of the electronics chip. Every Pixel Unit Cell (PUC) of the Readout Chip (ROC) contains 5 Static Random Access Memory (SRAM) cells. 4 SRAM cells are used for storing the trim bits and the fifth SRAM cell enables/disables the pixel. Enabling of e.g. noisy pixels is a problem, since entire Double Columns (DCOLs) could be lost. The worst case is the switching of memory cells in the global Digital Analog Converters (DACs). Consequently the SEUs are a potential danger to loose some vital detector control functions.

For investigation of the standard SRAM cell a simple shift register test structure was fabricated. Additionally a shift register with standard SRAM cells protected by a capacitor has been designed. The cross sections for both types of SRAM cells have been determined in a beam test with pions at PSI for different supply voltages. With a PSI46V1 chip exposed to a pion and proton beam the cross sections of the SRAM cells for SEUs in the real environment within the ROC have been also measured.

The SEU cross sections are decreasing with an increasing supply voltage. The benefit of the protection capacitor is depending on the switching direction about a factor of 100 in the cross section. For the ROC the pion cross sections for the unprotected SRAM cells are 2.42×10^{-14} cm^2/SRAM for a transition from 0→1 and 0.0115×10^{-14} cm^2/SRAM for a changeover from 1→0. In the case of the protected SRAM cells the cross sections are 2.57×10^{-16} cm^2/SRAM for the switching direction 0→1 and 0.529×10^{-16} cm^2/SRAM for changing the state from 1→0. The impact of 300 MeV/c pions compared to 500 MeV/c protons is about a factor of 4.7 worse. No indication for multiple bit upsets was observed.

For the correction of the SEUs the information has to be rewritten to the storage cells. This causes data traffic which is limited by the number of control links. With the measured cross sections the SEU rate per control link for the first and second layer is less than 0.03 Hz. This means that in average it will take about 8 hours for switching of 1‰ of all SRAM cells per control link. This results in about 1 SEU per second for the entire pixel detector barrel (48×10^6 pixels). Therefore reloading single pixel cells during data taking can be most likely avoided.

For the final design of the ROC PSI46V2 the SRAM cells protected with an capacitor are used in the PUCs and for the global DAC registers.

Chapter 6

Laboratory Investigations with Prototype Modules

So far all measurements in various beam tests and in the laboratory have been performed with test structures and a single readout chip. For this reason the ROC, bump bonded to a dedicated single ROC sensor, was glued on a special chip carrier. This Printed Circuit Board (PCB) was directly connected to the testboard. The multi purpose Testboard (TB) used allows the operation of the ROC with/without TBM or the module in various configurations (more details in Sect. 7.2). For operating the ROC with the Token Bit Manager chip, the TBM was mounted on a separate PCB introduced between chip carrier and the testboard. On this provisional setup the trace layout and therefore the performance like signal delays and crosstalk have not been investigated under realistic conditions. Investigating prototype modules and demonstrating that the up to date just theoretical design is really able to fulfill the requirements was an important milestone on the way to the pixel detector. The final design of the barrel module described in Chapter 3 includes all the changes necessary due to the results from the tests done with the prototype modules.

In Figure 6.1 a photo of one of the prototype modules is shown. It was the first attempt to operate an ensemble of 16 ROCs assembled to a module. The used PSI46V1 ROCs needed additional 4 capacitors for operation. Three for the decoupling and filtering of the supply power and one for suppressing the oscillations caused by a design error (Sect. 4.1). In this obsolete design the bondable capacitors were soldered on the base plate and connected to the ROCs by direct wire bonds. The old base plate designed for the PSI43 offers 6 pads for capacitors for each ROC. The ROCs have been bump bonded to a sensor of the final design. For the other components of the prototype module like the power cable, the Kapton cable, the HDI and the base plate precursor versions were used. The base plate was already cut for testing the mechanical stability in two stripes with the final width. A working TBM was not available at this time. Therefore the signal distribution was done passively by a temporary patch which was wire bonded. The missing TBM was no restriction since the testboard allows to have full control over the module. Even the beginning of the module readout was under control. The module readout is started by the appearance of the token signal at the first ROC of the module. Normally the token passage is autonomously initiated by the TBM (Sect. 3.1.3). Finally the missing TBM turned out to be an advantage for the crosstalk measurements. With the prototype modules the full functionality of a complete module has

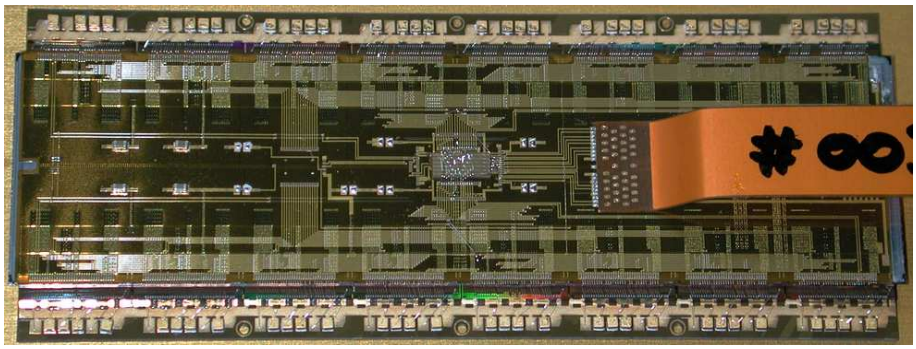

Figure 6.1: A prototype module assembled with 16 PSI46V1 ROCs and a final sensor. From the power cable, the Kapton cable, the HDI and the base plate preliminary versions are used. Since no TBM was available, the signal distribution was done by wire bonding. In this obsolete design, the capacitors for decoupling the power supplies of the ROCs were mounted on the base plate (compare Sect. 3.1).

been tested at the first time. In parallel to the commissioning of the prototype modules the testboard and the firmware for the FPGA[1] on it have been adapted and upgraded for the operation with a module.

Another aspect of the prototype module production was the test of the assembly line. The dedicated assembly line was set up for the mass production of the barrel modules [43]. Furthermore appropriate test procedures for partly assembled module components e.g. the bare ROC-sensor sandwich, the HDI equipped with passive components, the TBM and the signal/power cable etc. have been investigated.

6.1 Test Setup

The test setup for the crosstalk measurements in the laboratory consisted basically of a module operated by the testboard. To be as flexible as possible in the measurements the TB was operated in a mode that allows to use external control signals for the running operation of the module. The clock, trigger, calibrate and token signals were provided by a programmable pattern generator (Tektronix DG2020A). The commands for initializing all registers of the ROCs and programming various set ups of the module were delivered by a PC to the TB. Both, the TB with the FPGA and the pattern generator were controlled by this PC. The former via the parallel port and the latter by the SCSI interface. The power and the bias voltage for the module were also provided by the TB. The testboard fulfilled two functions which corresponds to the tasks of the control and readout system of CMS (Sect. 2.4.3).

The control commands for programming all the registers of the 16 ROCs on the module were written block by block via the parallel port into a shift register of the FPGA on the TB. Then the data were automatically transferred serially as a LCDS signal to the module synchronized by the external clock. The clock was also used for the operation of the FPGA.

[1] A field-programmable gate array or FPGA is a semiconductor device containing programmable logic components and programmable interconnects.

The other external signals from the pattern generator were directly connected to the Kapton cable of the module. The token was fed to the FPGA and to a counter to notify that a readout will start soon.

The serial readout of the 16 ROCs took place after sending a trigger and a token signal to the module. Since the analog pulse height was not available with the PSI46V1 (Sect. 4.1) a dedicated counter was implemented in the FPGA. The task of this counter was, to determine the length of the readout by counting the number of clock cycles. The counter was started with the token and stopped with the end of the readout sequence. The length of an empty readout of a module with 16 ROCs and without a TBM is 48 cycles (16×3 cycles). For every pixel hit 6 cycles are added (Fig. 4.4). Therefore this counter could be used for the determination of the number of hits in the readout. For many crosstalk measurements threshold scans were performed. Hence just the information of an empty or not empty readout was needed. Thus the missing analog pulse height was no limitation.

Before the measurements were performed, suitable settings for a stable operation of the 16 ROCs had to be found. According to the experience from chip testing the analog current of each ROC was adjusted to 24 mA. The internal regulated digital voltage is stabilized by one of the external capacitors. Therefore the voltage is accessible and was adjusted to 2.0 V for each ROC. The module was operated untrimmed since at this time no reliable trimming algorithm was available. Not trimmed means that the global threshold settings of the 16 ROCs were adjusted manually to get a roughly uniform threshold for the entire module. But the trim bits for the fine adjustment of the thresholds of all pixels were not used. With this simple approach it was possible to ensure a stable operation of the module. To get a uniform readout of the ROCs, the $V_{IbiasROC}$ and $V_{IbiasDAC}$ were adjusted. These two regulators are used for matching the pixel address ranges and the output levels. In Reference [69] a list of recommended values for several DACs of the ROC can be found.

As an example a complete readout of a module with 16 ROCs can be seen in Figure 6.2. In each ROC the same pixel gets the calibration signal. The second calibrate injection occurs after the readout of the 8^{th} ROC during the running readout belonging to the first calibrate pulse. Therefore the ROCs 9-15 have no second hit since the DCOL resets itself after a readout. This is one source of data loss (Sect. 7.3).

6.2 Crosstalk

The main cause of signal integrity problems in integrated circuits is noise induced by neighboring connections or crosstalk. In the CMOS technologies, this is primarily due to coupling capacitance, may be caused by charge injection into the substrate and at very high frequencies by mutual inductance. Concerning the readout chip the scope was on the power rails inside the chip. Therefore the connections of the $V_{substrate}$ (V_{well}) are kept separate from V_{ss} (V_{dd}) power rails to reduce the crosstalk in the ROC (Fig. 6.3). Induced noise can deteriorate the performance of a proper working device which design works in principle correctly. For example when the module of the pixel detector can only be operated at a high global threshold of 5000 electrons instead of a required threshold of 2500 electrons due to crosstalk.

In integrated circuits with analog and digital functions (called mixed-signal ICs) it is crucial to minimize noise coupling between various parts. The system can only work correctly

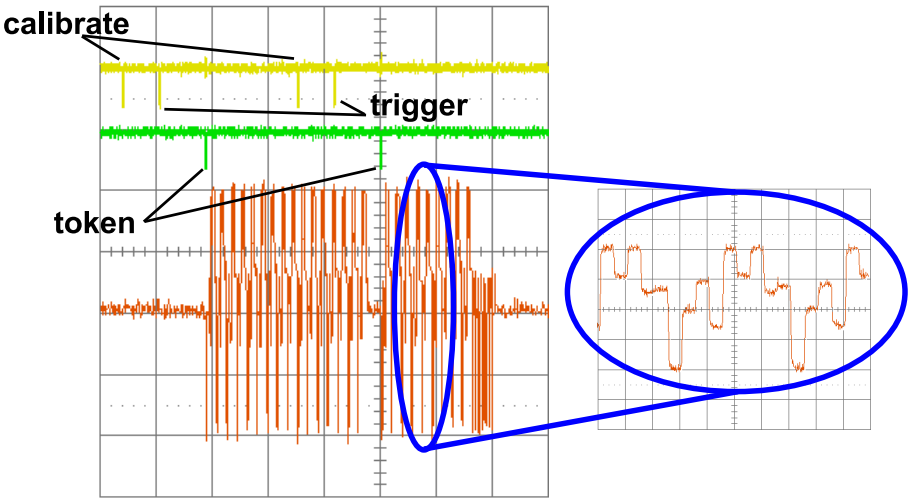

Figure 6.2: A complete readout of a module with 16 ROCs generated by a calibrate, trigger and token signal. In each ROC the same pixel gets the calibration pulse. The second calibrate pulse occurs during the readout of the first calibrate injection and therefore the ROCs readout after the second calibrate pulse did not have the second hit. After a readout the DCOL resets itself and the contents of the data buffers are deleted.

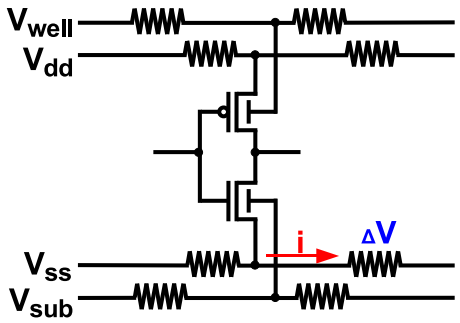

Figure 6.3: The $V_{substrate}$ and the V_{well} connections are separated from the V_{ss} and the V_{dd} power rails to suppress crosstalk in the ROC.

when the sensitive analog circuits and the noisy digital circuits can effectively coexist. The high-swing high-frequency noise injecting digital circuit may lead to undesired signal coupling to the sensitive analog circuit. To minimize the coupling via power rails, the analog and digital parts are supplied by separated V_{ana} and V_{dig} power rails. Another significant reason of signal coupling is the crosstalk between analog nodes themselves. The media through which mixed-signal noise coupling occurs is the substrate. The digital operations cause fluctuations in the underlying substrate voltage, which spreads through the common substrate causing variations in the substrate potential of sensitive devices in the analog section. In the case of crosstalk between analog nodes, a signal couples from one node to another via the substrate.

6.2.1 Intra Module Crosstalk

For the operation of the pixel detector it is crucial to keep the dead-time as little as possible, since it causes inefficiency. Therefore a major design goal of the ROC was to perform continuous data taking and simultaneous readout operation with minimal dead-time (Sect. 4.1). A consequence of this requirement is that the crosstalk caused by a running readout operation in the digital part of the ROC must be low in order to suppress distortion of data taking in the analog parts of the pixels or ROCs not involved in the readout. Crosstalk can occur in all phases of the readout operation. Possible sources for crosstalk are the running readout within the ROCs or the module.

Investigating the crosstalk on the module level includes all crosstalk sources on the ROC and DCOL level. The crosstalk generated on the HDI and the Kapton cable is also taken into account. Since the TBM was not available, this potential additional crosstalk contribution is missing.

6.2.1.1 Crosstalk within the readout chip

During a running column drain within a DCOL all pixels are sensitive for a further second or third hit besides the pixels initiated the current column drain (Sect. 4.1.1). The column drain runs through a DCOL with a rate of about 3.3 GHz corresponding to 0.3 ns per pixel. The column readout token stops at each pixel with a hit for transferring in parallel 9 digital address bits and the analog pulse height to the periphery. For this procedure the switching of several transistors in the PUC is needed. Hence it can cause crosstalk to other pixels in the neighborhood and may create fake hits. The distorted pixels can be in the same DCOL or in consecutive ones. The spurious hits can be generated by increasing the pulse heights of real particle signals artificially above the comparator thresholds or by lowering the thresholds of the comparators temporarily causing noise hits. The effect of the fake hits depends on its number. Just a few additional hits increase the time needed for the column drain or causing additional column drains in other DCOLs. Therefore the dead-time and inefficiency will be increased. A more serious problem is the lowering of the threshold. It can generate many noise hits overflowing the data buffers and reseting the DCOLs. In this case the permanent operation of the pixel system at the given threshold might be impossible. Hence the threshold of the system has to be increased to guaranty continuous data taking and simultaneous readout operation. A higher threshold causes a worse spatial resolution and a higher inefficiency. The contrary effects of lowering the pulse heights and increasing the thresholds by crosstalk can also occur. But the consequences are less serious, since a higher threshold decreases the efficiency just temporarily and keeps the system still working properly.

The readout of triggered events from a ROC, controlled by a external token initiated by the TBM, can generate crosstalk too. Since this operation is restricted to the DCOL periphery and the global part of the ROC, less crosstalk to the sensitive pixel array is expected. The crosstalk within the ROC can be transmitted by substrate coupling or capacitive coupling. Within a DCOL especially the bus structure of traces running along the DCOL for connecting the pixels with the DCOL periphery and the power rails are also a possible media for crosstalk.

6.2.1.2 Crosstalk within the module

The readout of the ROCs of a module happens in a daisy chained way (Sect. 3.4). Hence it is possible that the activity due to the readout in one ROC produces crosstalk to other ROCs of the module. The coupling may happen, because of the sandwich structure of the module, via the sensor or via the HDI. All control signals on the HDI can couple to other traces and may be responsible for crosstalk. The HDI is also the place for crosstalk created by ripple on the digital and analog power supply voltage. The ripple may be generated by ROCs with a transitionally higher activity during readout operation. The fluctuating power consumption causes voltage drop variations due to the ohmic resistance of the power lines and the ground grid on the HDI. Since all ROCs are supplied in parallel with power by the HDI this ripple is transmitted to the other ROCs. To suppress high frequent ripple from the ROCs to the HDI and to buffer high frequent power variations on the HDI the power of the ROCs is decoupled by capacitors mounted next to each ROC. For low frequency distortions with a duration more than about 50 ns the on chip regulators respond to the variations (Sect. 4.1.3).

6.2.2 Measurements and Results

For the crosstalk measurement 15 ROCs of the module are programmed with a trigger latency of the value *latency_1*. The latency is the number of clock cycles how long the ROC stores locally the pulse heights and the pixel addresses. When the latency is passed the hits confirmed by a trigger are read out. The not confirmed hits will be discarded (Sect. 4.1.2). In these 15 ROCs a number of pixels are enabled and prepared to get a calibrate injection by the internal mechanism of the ROC. The calibrate mechanism is initiated by the external calibrate pulse from the pattern generator. After the calibrate injection the column drain mechanism is started in each DCOL containing pixels with hits. The length of the column drain depends on the number of pixels which got a calibrate signal. For the ROCs with *latency_1* no appropriate trigger signal is supplied from the pattern generator. Therefore in these ROCs the content of the data and time stamp buffer is discarded after *latency_1* is passed. The 16^{th} ROC gets a longer *latency_2* and only one test-pixel is enabled. This test-pixel gets no calibrate injection. But the 16^{th} ROC receives an appropriate trigger signal to its *latency_2*. After the token signal is given by the pattern generator the readout of the module starts. Since the *latency_1* is already passed, the 15 ROCs with *latency_1* have no trigger confirmed hits. If applicable only the test-pixel of the 16^{th} ROC is read out. This pixel got no calibrate signal. Thus the read out hit has been caused by crosstalk from the other activities on the module or by noise. To make this measurement more sensitive a threshold scan with the test-pixel is performed. The achieved s-curve is then fitted with an error function and the position of the 50 % point is extracted. In the case of the PSI46V1 the threshold scans are important since no analog pulse height is available. For investigations of the crosstalk at different stages of the column drain mechanism the trigger position for the test-pixel is varied with time. At each position a threshold scan is performed with the test-pixel. The baseline for this investigations is taken by sending the calibrate pulse without any pixels enabled in the 15 ROCs. Doing this the intra module crosstalk can be quantified at any stage of the column drain mechanism and even before the column drain is started.

For clarification of the following measurements given with an absolute threshold one has

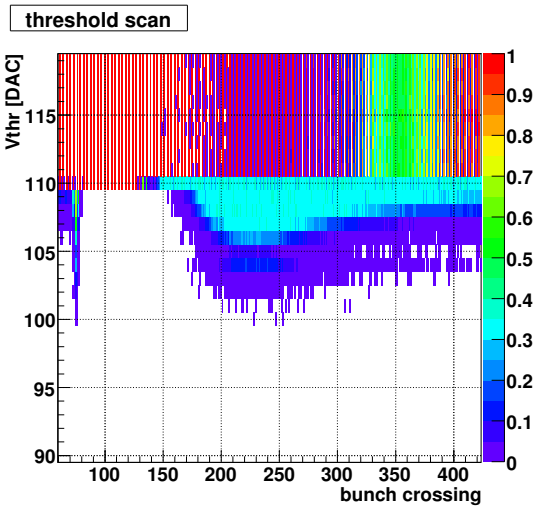

Figure 6.4: Crosstalk caused by a running column drain. A threshold scan using a test-pixel was performed at each position. The setting up of the column drain causes a positive pickup and during the running column drain a negative pickup was observed.

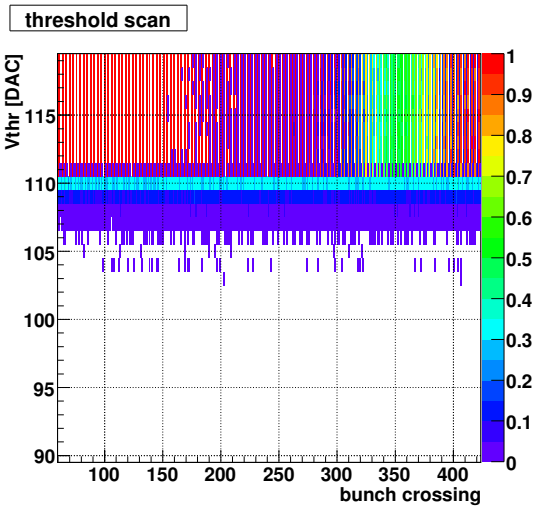

Figure 6.5: To quantify the crosstalk a baseline measurement was performed. Therefore no pixels were enabled in the 15 ROCs. The efficiency is color coded.

to note that V_{thr} DAC is inverted: a high DAC value corresponds to a low threshold. For too high V_{thr} values the signal disappears and the pixel is in an unstable operation mode (e.g. in Fig. 6.4 and Fig. 6.5). The reason for this is that the threshold falls below the noise and the pixel stops working properly. The crosstalk investigations of the column drain mechanism can be divided in two phases. The crosstalk caused by starting the column drain mechanism and the crosstalk caused by a running column drain.

The column drain mechanism is started after the calibrate injection. In Figure 6.4 the calibrate pulse occurred in clock cycle 72. Immediately after the calibration pulse a spike of positive pickup can be seen caused by setting up the column drain mechanism. During the running column drain a negative pickup was observed. A corresponding baseline scan is shown in Figure 6.5. A positive pickup means that the threshold is lowered or the pulse height of the signals is increased temporarily and for negative pickup vice versa. The relative threshold shift caused by crosstalk from starting up the column drain mechanism is shown in Figure 6.6. This graph was gained by performing for several scenarios and V_{IColor} values a scan and subtracting the baseline in the region of the positive pickup after the calibration pulse. The threshold shift is plotted versus the V_{IColor} DAC value. The V_{IColor} regulator limits the current for the double column periphery notification. For an unrealistic scenario of 20 pixels per column in all columns of the 15 ROCs the measured threshold shift is in the range of 3.5 DAC values of V_{thr} corresponding to about 770 electrons[2]. This value is

[2]The calibration factor of 220 electrons/DAC_step of V_{cal} has been determined with X-ray sources in the laboratory. K_α lines of 6 different isotopes between 8.04 keV and 44.2 keV have been used [84]. With threshold scans for several V_{cal} values the translation of V_{cal} to V_{thr} was performed. One DAC step of V_{thr} corresponds to about 220 electrons. Due to some design changes this calibration is only valid for PSI46V1.

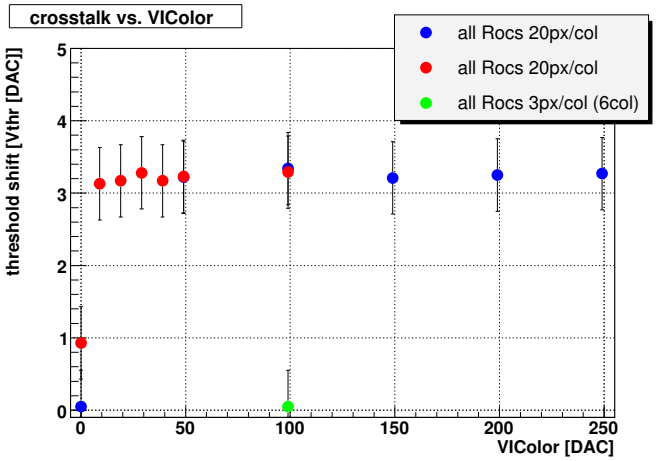

Figure 6.6: The set up of the column drain causes a threshold shift of about 770 electrons for a unrealistic scenario of 20 enabled pixels in each column of the 15 ROCs. For a realistic cluster size of 6 columns, in each 3 pixels enabled, the effect is less than 40 electrons.

independent of the V_{IColor}. For a realistic cluster size of 6 columns per ROC, each having 3 pixels enabled, the crosstalk is less than 40 electrons.

To investigate the negative pickup of the running column drain mechanism, the single test-pixel with *latency_2* got a calibrate injection. Thus the test-pixel is moved away from the noise level. By doing this, the method got sensitive for negative pickup. Without this calibration pulse the test-pixel is already in the noise due to the lowered threshold and quantification of the negative pickup is not possible. In Figure 6.7 the equivalent crosstalk measurement like in Figure 6.4 is shown where 20 pixels in each column in 15 ROCs are enabled. The distortion in the range of the clock cycles higher than 300 is an artifact of the pattern generator. The corresponding baseline measurement is shown in Figure 6.8 with no pixels enabled. Since the calibration mechanism of the ROC needs some clock cycles between two consecutive calibrates for regeneration, the scans start after the first calibrate injection. The positive pickup after the calibrate pulse is partly caused by the recovery of the calibration mechanism and partly by activity in all PUCs analog part. Despite disabling the pixels the calibrate signal which is lay outed to each PUC couples to the them and cause activity. Disabling a pixel means only that the pixel can not initiate the column drain mechanism since the "Hit FF" is blocked by the mask bit (Fig. 4.2). The rest of activity is not suppressed in the PUCs. Subtracting the baseline from the thresholds one gets the relative threshold shifts related to the running column drain (Fig. 6.9). The length of the negative pickup corresponds to the length of the running column drain. The case where 20 pixels per column have been enabled is shown in Figure 6.7. That means 40 pixels per DCOL. The column drain mechanism needs in average 2 clock cycles per pixel for transferring the data to the data buffer (Sect. 4.1.2). Therefore a negative pickup of about 80 cycles is expected which can be seen in Figure 6.9. For 10 enabled pixels per column for all ROCs the result can be seen in Figure 6.10. The length of the column drain is about 40 clock cycles. The value of the negative threshold shift is for both cases about 2000 electrons complying with a change of about 50 % of the threshold. For a more realistic scenario of 10 pixels in two columns in 15 ROCs the resulting plot is shown in Figure 6.11.

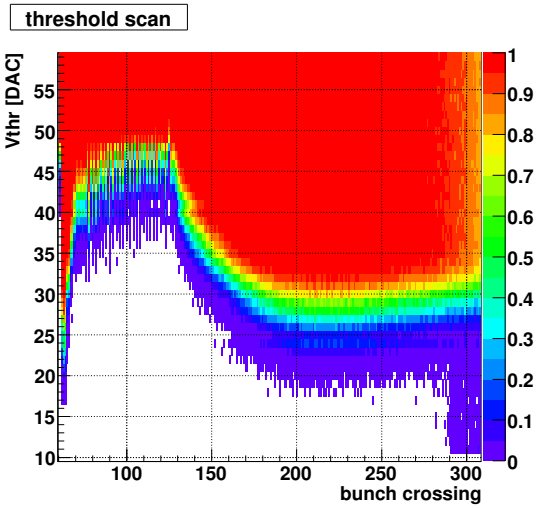

Figure 6.7: Negative pickup caused by a running column drain. The length is related to the length of the column drain and therefore to the number of hits per DCOL. The test-pixel is moved away from the noise level with a calibration pulse.

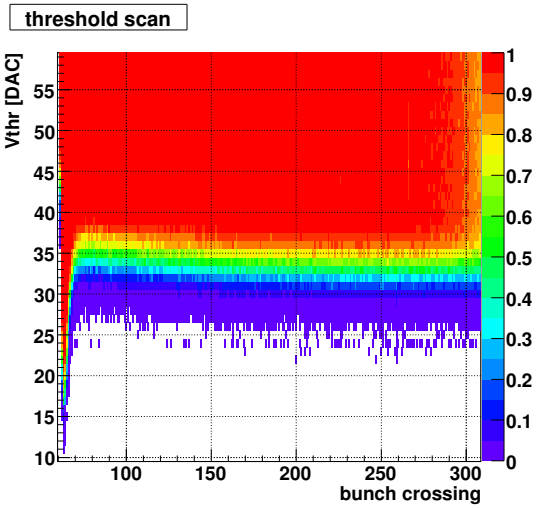

Figure 6.8: The baseline measurement was performed without any enabled pixels. The positive pickup is caused by the activity in the analog parts of all PUCs after a calibration pulse (see text). The efficiency is color coded.

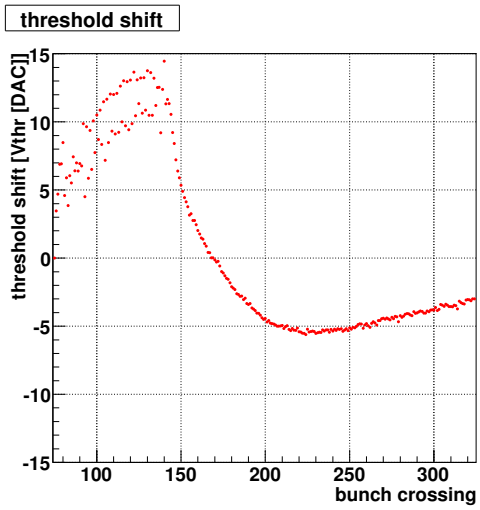

Figure 6.9: Threshold shift for a running column drain with 20 pixels per column in 15 ROCs enabled. The length of the column drain is about 80 clock cycles corresponding to the length of the negative pickup. The shift is in the range of 2000 electrons.

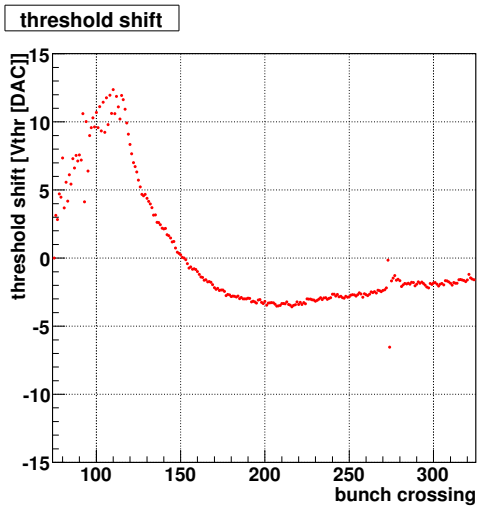

Figure 6.10: Threshold shift for a running column drain with 10 pixels per column in 15 ROCs enabled. The length of the column drain is about 40 clock cycles corresponding to the length of the negative pickup. The effect is in the range of 2000 electrons.

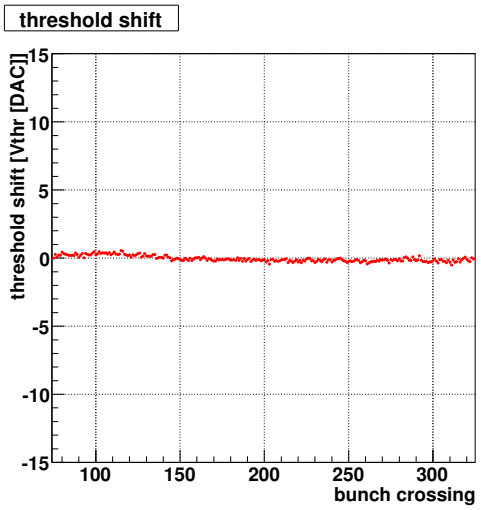

Figure 6.11: Threshold shift for a running column drain with 10 pixels in 2 columns in 15 ROCs enabled. For this realistic scenario the pickup is negligibly.

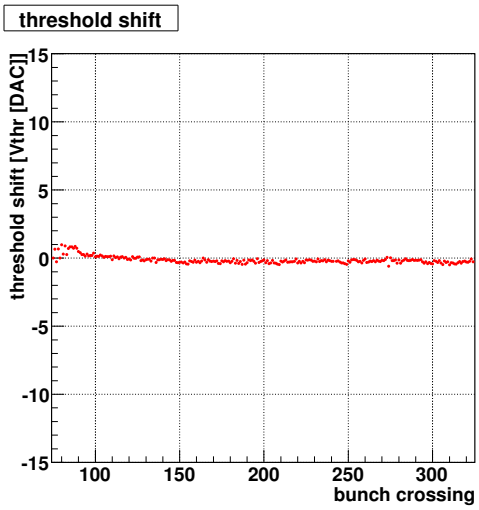

Figure 6.12: Threshold shift for a running column drain with 3 pixels in 6 columns in 15 ROCs enabled. For this realistic cluster size the pickup is about 200 electrons.

For 3 pixels per column in 6 columns per ROC corresponding to a realistic cluster size the result is shown in Figure 6.12. In the case of realistic scenarios the change of the threshold caused by running column drains is less than 200 electrons.

For heavy ion collisions the number of charged particles produced in Pb-Pb collisions at $\sqrt{s_{NN}} = 5.5$ TeV is in the range of 8000 particle per unit of pseudorapidity [5]. With a mean radius of 44.4 mm and 18 faces for the innermost layer of the pixel detector with a module length of 66 mm the averaged number of tracks per ROC is approximately 37. Therefore the number of tracks per DCOL is about 1.4 which results in 3 pixels per DCOL with a averaged pixel multiplicity of 2.2. Assuming a linear extrapolation of the measured crosstalk during the startup of the column drain mechanism, a threshold shift of about 100 electrons is expected. For the running column drain the crosstalk is estimated to be in the range of about 300 electrons. Under the assumption of a pixel detector threshold of 2500 electrons, the crosstalk seems to be even for heavy ion collisions reasonable.

Besides the column drain mechanism the readout operation may cause crosstalk. Since the ROCs are read out serially, all pixels are sensitive for pickup during a running readout on the module. To investigate the crosstalk of a running readout operation the module was setup like in the measurements for studying the crosstalk during a column drain. In addition, the ROCs with *latency_1* got a appropriate trigger signal and therefore the hits have been confirmed. To restrict the length of the adjacent readout only one pixel of one ROC got a calibrate injection. This restriction has no influence on the result, since the readout is serially. After the token has arrived at the first ROC the serial readout of the module was started. The readout length in this configuration was 16×3 clock cycles for the empty readout plus 6 cycles for the pixel which got the calibrate injection. The test-pixel got no calibrate pulse. By scanning the trigger and the token signal for the test-pixel over the period of the readout of the other ROCs, the crosstalk in each phase of the readout could be investigated. At each

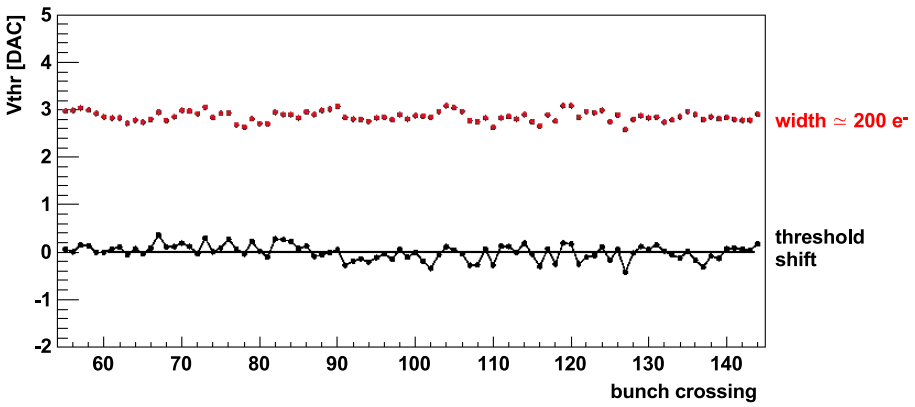

Figure 6.13: Crosstalk during a running readout operation on the module. There is no significant pickup in the test-pixel during the readout and the adjacent data buffer reset. The upper curve shows the slopes of the s-curves which are related to the noise (see text).

position a threshold scan with the test-pixel was performed. In Figure 6.13 the threshold shifts are shown. The readout of the 16 ROCs starts in bunch crossing (bc) 62 and ends in bc 116. No significant pickup during the running readout compared to the bunch crossings before the readout started can be seen. After the readout of the hits of a DCOL the buffers are immediately reseted. During the reset of the DCOL in the range of bunch crossing 120 no crosstalk was observed. In addition to the relative threshold shifts the slopes of the s-curves, gained with the error function fits, are plotted. The slope (width) is related to the noise. A constant slope is an indication that there was no additional noise induced by the readout activity on the module.

The initial motivation for the crosstalk investigation was the question if continuous data taking and simultaneous readout operation is possible at a reasonable low threshold. The design goal for the operation of the pixel detector is a threshold of 2500 electrons [68]. The performed measurements showed that the developed method is sensitive for investigating the intra module crosstalk. For a realistic cluster size the threshold is shifted temporarily less than 40 electrons by a positive pickup at starting up the column drain mechanism. During the running column drain the threshold shift is in the range of 200 electrons due to a negative pickup. Therefore the contributions from starting up the column drain mechanism and the adjacent column drain is negligible. The readout operation and the adjacent reset of the DCOLs cause no significant additional pickup.

6.3 Token Passage on the Module

A crucial requirement for the design of the High Density Interconnect was to keep the capacitive load of the traces as low as possible. The load is responsible for the generation of the timing skew of the signals. To investigate the timing of the signals, measurements with a prototype module equipped with a preliminary version of the TBM (TBM04), were done. For the control signals, distributed from the TBM to the branches of 4 ROCs, the timing is acceptable. A serious concern was always the timing of the token signal. It is the most critical

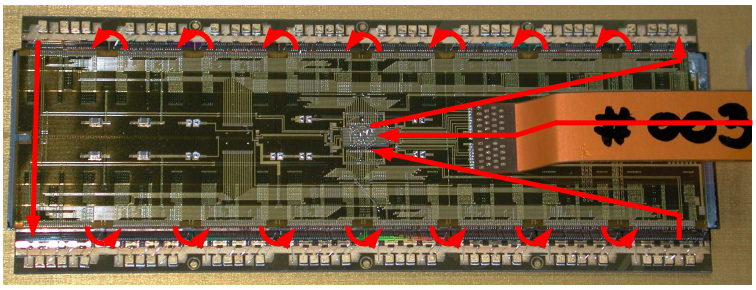

Figure 6.14: Token passage on a prototype module. Indicated is the token passage for a module of layer 3.

control signal for the operation of the module. If the token gets lost, the module is blocked until the next reset. Due to the readout scheme of the module (Sect. 3.4) the token is sent from the TBM to the first ROC (Fig. 6.14). The ROC transmits the token to the next ROC after finishing the readout to the corresponding trigger. The token leaves the ROC with the falling edge of a clock cycle and it is recognized at the input of the consecutive ROC with the rising edge of the clock signal. Therefore the propagation time should be less than 12.5 ns (half periodic time of 40 MHz). In the case of the token passage from ROC 0-7 and from the ROC 8-15 within a row of ROCs on the module the timing is sufficient.

The most critical section of the token passage is from ROC 7 to ROC 8. This passage is only necessary for modules of the third layer. The modules of layer 1 and 2 are read out by two analog optical links (Sect. 2.4.3 and Sect. 3.4). For this reason the token_out signal from ROC 7 is routed back to the TBM. The second analog optical link reads out the ROCs 8-15. Therefore the token is sent from the TBM in dual mode to ROC 8. Requiring for the two types of modules only one HDI design, the preliminary HDI_V2 version has the possibility to connect directly the token_out signal of ROC 7 to the token_in pads of ROC 8. The configuration is done by wire bonds. In addition the token traces lay outed from ROC 7 to the TBM and from the TBM to ROC 8 for dual mode operation are acting as capacitive load anyhow. Therefore the token output amplifier of ROC 7 has to drive in the single mode operation in total a measured capacitive load of about 21 pF. According to simulations of the token output amplifier in combination with the token receiver of PSI46V1 (Fig. 6.15) the delay with this load is already in the range of 11 ns which is too tight. The measurements with the prototype module have confirmed this concern. With an operation clock frequency of 10 MHz and 20 MHz no problem was observed. With 40 MHz clock frequency one clock cycle was lost during the transfer of the token from ROC 7 to ROC 8 (Fig. 6.16). The data read out from the module are transmitted to the Front-End Driver. This unit expects apart from the TBM header and trailer, that an empty readout from the module consists of 48 cycles for 16 ROCs plus a multiple of 6 cycles for every additional pixel hit. If there are sometimes extra clock cycles in the readout sequence the FED may run in problems concerning the recognition of the data stream.

To avoid this problem a faster version of the token transmitter and receiver have been designed and implemented in the PSI46V2 chip. The delay of these stages for different capacitive loads is shown in Figure 6.15, too. For a capacitive load of 21 pF the delay is

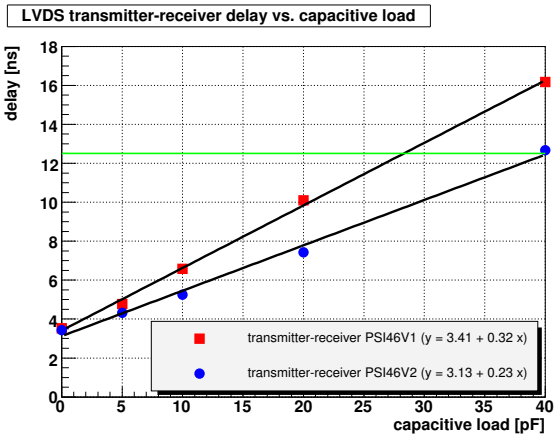

Figure 6.15: The LVDS transmitter - receiver delays for various capacitive loads. The design of PSI46V1 has for a capacitive load of 21 pF a delay of about 10.5 ns. The faster version of PSI46V2 has for 21 pF a delay of about 8 ns.

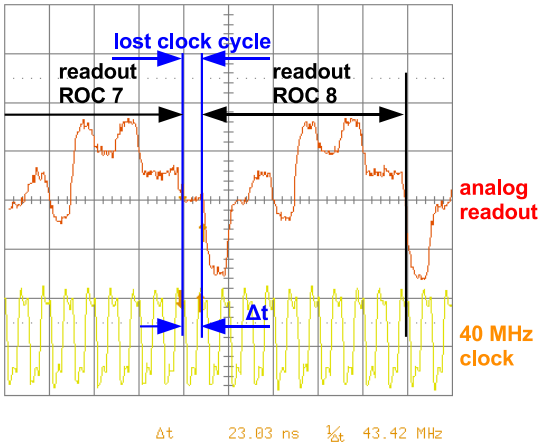

Figure 6.16: On the token passage from ROC 7 to ROC 8 a clock cycle is lost with a clock frequency of 40 MHz.

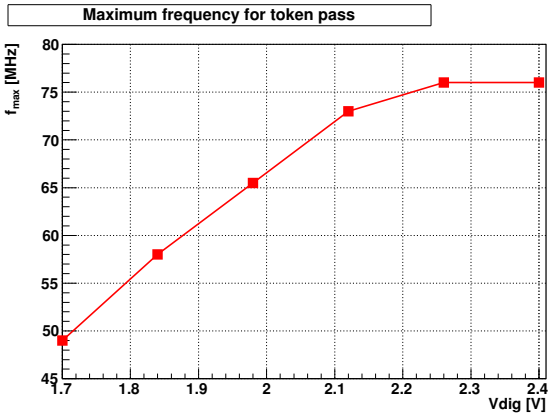

Figure 6.17: The maximum clock frequency for token passage on a module with the final HDI_V3 and the new transmitter and receiver implemented in the ROC PSI46V2 as a function of the digital voltage. At a nominal V_{dig}=2 V the module works up to a clock frequency of 65 MHz.

expected to be about 8 ns. The maximal achievable clock frequency without loosing a clock cycle on the token passage from ROC 7 to ROC 8 with the PSI46V2 and the final design of the HDI_V3 was measured as a function of the digital voltage (Fig. 6.17). For the lowest V_{dig} of 1.7 V the token passage works up to 48 MHz. For the nominal digital voltage of 2.0 V the token transfer works up to a clock frequency of 65 MHz. With the new designed transmitter and receiver stages of the PSI46V2 ROC there was sufficient margin in the token timing for reorganizing the token layout of the module.

On the prototype HDI_V2 it was foreseen to connect the token_out of ROC 7 with wire

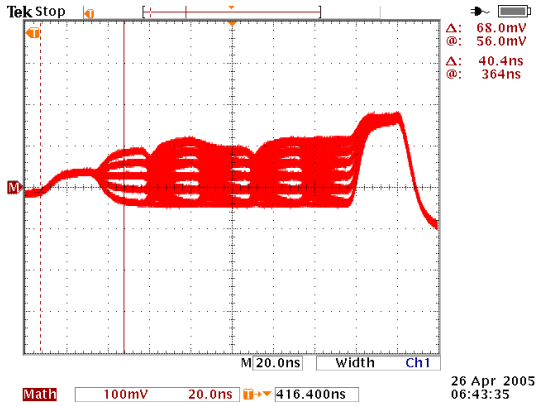

Figure 6.18: Superposition of the analog readouts for all pixels of a ROC at 40 MHz measured after the Kapton cable. The level separation for high address levels is 50 % smaller than for the levels 0 and 1.

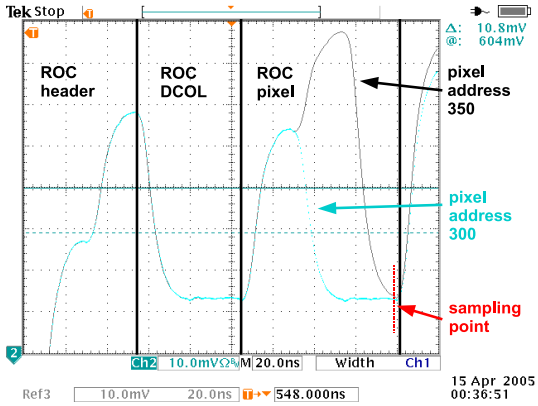

Figure 6.19: Superposition of two readouts with different pixel addresses (pixel address 350 and 300). There is no margin for the sampling point left.

bonds directly to the token_in of ROC 8 for a module of layer 3. To avoid this time consuming approach and to get more flexibility in exchanging the modules between different layers the wire bond possibility was removed from the final HDI_V3. A secondary effect of removing the wire bond pads was the lowering of the capacitive load of the token traces. In the case of a final layer 3 module with a TBM working in the single mode operation the token from ROC 7 is transmitted to the TBM and is sent to the ROC 8 with a total time delay of less than 12.5 ns. Therefore switches in the TBM for passive token passage are configured in the single mode operation. This feature was implemented in the final TBM (TBM05) version. The benefit of this new token layout is that all modules for the barrel part are assembled in the same way. These standard modules will be (re-)configured by software according to their final position in the barrel detector.

6.4 Analog Chain of the Module

The capacitive load of the traces on the HDI is not only an issue in the case of the token passage. The analog chain of the module contains the 4 ROCs of a branch, the traces from the ROCs to the TBM on the HDI, the TBM and the traces from the TBM to the Kapton cable (Sect. 3.1.4 and Sect. 3.4). In Figure 6.18 the superposition of the analog readouts for all pixels of a ROC at 40 MHz is shown. It was measured after the Kapton cable. A marginal level separation for high address levels was observed. Depending on the ROC settings, the separation between address levels 4 and 5 is about 50 % smaller than between level 0 and 1. Since the ROC showed no linearity problem the level separation was related to the amplifiers in the TBM04. By redesigning these amplifiers the linearity problem has been solved.

In addition to the linearity problem of the analog chain a speed problem was discovered. In Figure 6.19 two analog readouts of two different pixels (pixel address 350 and 300) are superimposed. Depending on the sampling point, there is a level shift caused by the previous address level. With the components used for the prototype module (PSI46V1 and TBM04)

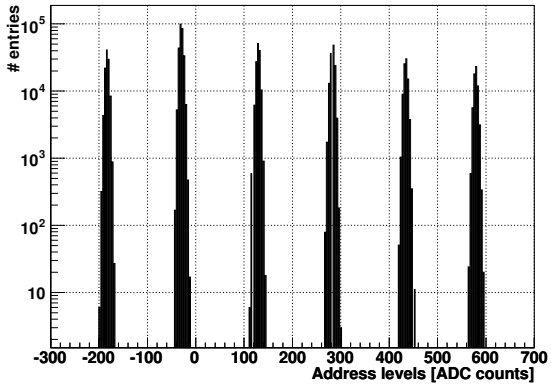

Figure 6.20: The module address levels are clearly separated with the improvements of the TBM05 (compare Fig. 6.18).

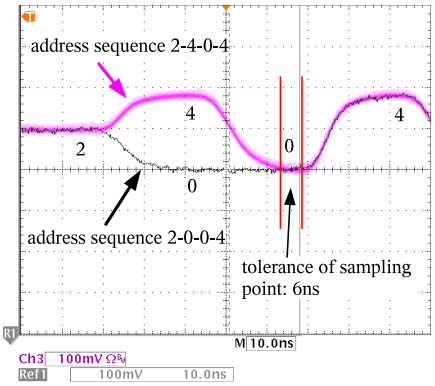

Figure 6.21: Readout signal of an improved barrel module (PSI46V2 and TBM05) for two different address sequences (2404 and 2004). The tolerance for the sampling point is about 6 ns (compare Fig. 6.19).

there is no tolerance left concerning the sampling point. The analog chain can be regarded as a chain of RC filters consisting of the ROC, the HDI, the TBM and the Kapton cable. Each stage by itself is fast enough, but the sum of all is too slow and causes the speed problem. To solve the speed problem each stage of the analog chain was investigated. The ROC internal rise-time was measured to be in the range of 2.0 ns. Since the rise-time at the analog input of the TBM was about 3.3 ns the input termination was changed from 270Ω to 135Ω resulting in a rise-time of 1.9 ns. The TBM internal rise-time for the analog signal was improved from 2.2 ns to 1.1 ns by redesigning the amplifiers. Additionally the capacitive load of the traces on the HDI have been minimized for the final HDI_V3 design.

After all the linearity problem and the speed problem of the analog chain have been solved by redesigning the analog chain of the TBM and by optimizing the HDI. The results of these improvements concerning the level separation are shown in Figure 6.20. Compared to Figure 6.18 the linearity is clearly advanced. The speed of the improved analog chain can be seen in Figure 6.21. With the redesigned components the margin for the sampling point is in the range of 6 ns at the output of the module compared to the "zero tolerance" in Figure 6.19. The measurement with the new components were performed at the output of a module with the ROC version PSI46V2 and a TBM05.

6.5 Summary

A major requirement for the pixel detector is to perform continuous data taking and simultaneous readout operation with minimal dead-time and a maximal efficiency. Therefore the crosstalk caused by activity in some parts of the Readout Chips (ROCs) or module during data taking has to be minimal to avoid distortion of the sensitive parts of the ROC. The main activities during data taking is the column drain mechanism, which copies the data from the active pixel array down to the double column periphery, followed by the readout of

the triggered events.

A method to investigate the intra module crosstalk was developed. Crosstalk for simultaneous column drain in large fractions of a module has been observed. During the start up of the column drain mechanism positive pickup was measured which caused a threshold shift for realistic cluster sizes in the range of about 40 electrons. The running column drain caused a negative pickup. The threshold shift related to this negative pickup is for realistic scenarios about 200 electrons. For heavy ion collision the threshold shift for starting up the column drain mechanism was estimated to be about 100 electrons and for the running column drain mechanism approximately 300 electrons. The readout of the 16 ROCs in a daisy chained way causes no observable crosstalk. Concerning a global threshold of 2500 electrons the measured pickup caused by the column drain mechanism and the readout operation of the module is negligible.

The traces of the High Density Interconnect (HDI) are capacitive loads which are causing timing skew of the signals. One of the most important control signals is the token which is transmitted from ROC to ROC during the readout of the module. With the investigated prototype modules one clock cycle was lost on this passage with an operation clock frequency of 40 MHz. With the design modifications of the transmitter and receiver of the token implemented in the ROC PSI46V2 the token passage works until a clock frequency of 65 MHz at nominal digital voltage.

Another problem concerned the analog readout chain of the module. Due to a linearity problem the address level separation was insufficient. Combined with the linearity problem a speed problem of the analog readout has been seen. By optimizing the capacitive loads of the traces on the HDI_V3 and redesigning the analog amplifiers of the Token Bit Manager (TBM) chip both problems could be solved. With the redesigned TBM05 and HDI_V3 a margin of about 6 ns for the sampling point of the address levels is available.

All required improvements of the components of the module are implemented in the final design of these components.

Chapter 7

Module Beam Test under LHC like Conditions

Before the start of the mass production of the 800 modules for the pixel detector, the final version of the modules had to be tested under LHC like conditions. The goal of the beam test was to operate the test module in a mode of continuous data taking and simultaneous readout operation in a realistic high rate beam. One of the most interesting questions concerning the performance of the front-end has always been the inefficiency of the module under high track densities. For the investigations of the inefficiency the high rate environment is absolutely crucial since e.g. the limited number of data and time stamp buffers per double column in the ROC (Sect. 4.1.2) becomes only a noticeable restriction for the performance of the front-end in the case of high track densities. In addition to the high rate the measurements were performed with randomly triggered events to cover all statistical effects. So far all investigations in the laboratory were done with the calibrate mechanism. These hits and triggers are periodic and deterministic. Therefore it is not possible to cover with these hits all effects e.g. data buffer or time stamp buffer overflows (Sect. 4.1.2) which will appear only in high track density events. The design decisions affecting the readout architecture of the ROC and the module are based on simulations. Especially the expected inefficiency caused by the data losses resulting from the chosen design of the ROC and the TBM have been estimated with a dedicated algorithm simulating the readout architecture (Sect. 7.3). Till now just single ROCs without the TBM have been tested in high rate beam tests [65, 67]. It was the first time that a complete final module was operated under CMS like conditions.

The CMS environment in the region of the pixel detector can be characterized by the following parameters (compare Chap. 2):

- The bunch crossing frequency is 40 MHz resulting in a time of 25 ns between two consecutive bunch crossings.

- The track density is expected to be up to 40 MHz/cm^2 for high luminosity operation (10^{34} cm^{-2}s^{-1}). The highest fluence occurs at the radius of the innermost layer under the impact of the 4 T magnetic field for $\eta = 0$.

- The Level-1 Trigger (L1T) rate is estimated to be up to about 100 kHz.

- The minimal time delay between two consecutive triggers is two clock cycles corresponding to 75 ns from edge to edge of the trigger signals.
- The angle between the particle traces and the surface of the modules will vary since the pixel detector covers a range of $|\eta|$ <2.5.
- The operating temperature will be about -10 ℃.

The beam test took place at the πE1 beamline [86] at the Paul Scherrer Institut in 2005. Pions (π^+) with a momentum of about 300 MeV/c were used. The deposited charge for these particles in the Si sensor with a thickness of 285 µm is about one MIP corresponding to 23 ke$^-$ (Sect. 3.2.1). The bunch structure at the PSI accelerator complex is 50 MHz, but the test setup was operated with a synchronized 40 MHz clock frequency. The beam intensity corresponding to the track density was variable up to 150 MHz/cm^2. In contradiction to the CMS experiment there was no magnetic field applied and the module was operated at room temperature.

7.1 Module used in the Beam Test

After the measurements with the prototype modules in the laboratory (Chap. 6) the required changes to the components of the module have been implemented. The improvements have concerned the ROC, the TBM, the HDI, the Kapton cable, the power cable and the base plate. The current version of the modules was assembled with the final components. These are the ROC PSI46V2, the TBM05, the HDI_V3, the final versions of the Kapton cable, the power cable and the base stripes. The PSI46V2 ROC is described in detail in Chapter 4. The other final components and the design of the module are explained in Chapter 3.

For the beam test investigations a trimmed module was used. The goal of the trimming is to obtain a uniform response of all pixels over a module by setting the comparator thresholds of all pixels. The global comparator threshold of a ROC is set by the V_{thr} DAC. To compensate the local transistor mismatch a fine adjustment of the pixel threshold with the 4 trim bits per pixel unit cell is performed (Sect. 4.1.1). The trim bits allow 16 trim states. The effect of the trim bits is defined by a trim voltage, which is set globally per ROC with the DAC V_{trim}. By setting trim bits the threshold of the pixel is decreased. The input parameter for the trimming algorithm is the absolute physical threshold at which the response is to be unified. For practical reasons this threshold corresponding to a certain number of electrons has to be converted in V_{cal} DAC units which defines the height of the internal calibration pulse. The conversion factor from electrons to DAC units of V_{cal} is for the used ROC PSI46V2 about 65 electrons. This value was determined by measurements similar to them described in Section 6.2.2. The trimming algorithm for the module starts with this fixed V_{cal} and looks for the threshold distribution of the untrimmed module. Therefore a threshold scan with each pixel is performed. The widths of the raw threshold distribution of the ROCs define the V_{trim} DAC values for each ROC individually. The global V_{thr} DACs of the ROCs are set to the highest thresholds since by trimming the thresholds can only by decreased. After the trimming a threshold distribution by scanning the V_{cal} is performed. The distributions for the trimmed and untrimmed module are shown in Figure 7.1. For more details about the trimming algorithm see Ref. [68].

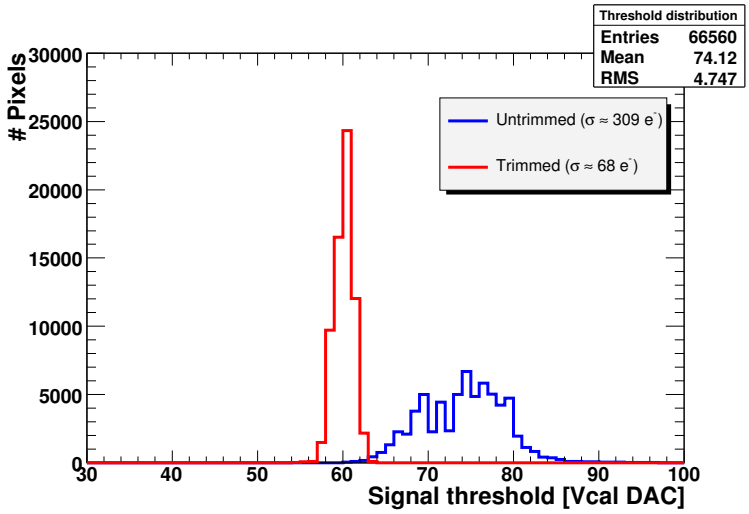

Figure 7.1: Trimmed and untrimmed pixel threshold distribution for the module. The width of the threshold distribution is improved by a factor of 4.5 by trimming. The absolute physical threshold to which the response was unified is about 3900 electrons.

7.2 Setup of the Beam Test

A schematic overview of the entire test setup for the module beam test including the Data Acquisition (DAQ) and the control and readout system is given in Figure 7.2. The beam telescope with the module and the tube containing the scintillator and the Photomultipliers (PMs) for triggering are shown in Figure 7.3.

The main components of the setup are the test module and the beam telescope. The beam telescope provides the information to reconstruct the tracks traversing the test module. For the efficiency investigations only tracks were taken into account which appeared in all 4 ROCs off the telescope. The other tracks may have caused a trigger but have not passed the module due to the beam divergence or multiple scattering[1] in the ROCs of the telescope. The module has a power dissipation of about 2 W and a mass of 2.2 g. For protection against overheating the module was mounted on a water cooled aluminum block which has stabilized the temperature at about 20 °C. The cooling structure was supported tiltable to emulate various angles from 0° to 90°. The final angle for operating the module depends on its position on the barrel of the pixel detector. The direction of 90° corresponds to an incident beam perpendicular to the surface of the module ($\eta = 0$) and 0° means that the module surface is in parallel to the beam. The module was controlled and supplied by the Module Testboard (MTB). The beam telescope is in principle a special module with 4 ROCs, each bump bonded to a dedicated single ROC sensor. The ROC sensor sandwiches were glued on separate chip carriers and plugged in the telescope PCB. This PCB is the mechanical support structure for the telescope and replaces electrically the HDI. It distributes the control signals and the power to the ROCs. Additionally it is equipped with a TBM for controlling and reading out

[1] With equation 2.11 one gets for ~ 1 mm silicon (750 µm ROC plus 285 µm sensor) and 300 MeV/c pions with $X_0 = 9.36$ cm for silicon a scattering angle of $\sigma_\Theta = 4.4$ mrad.

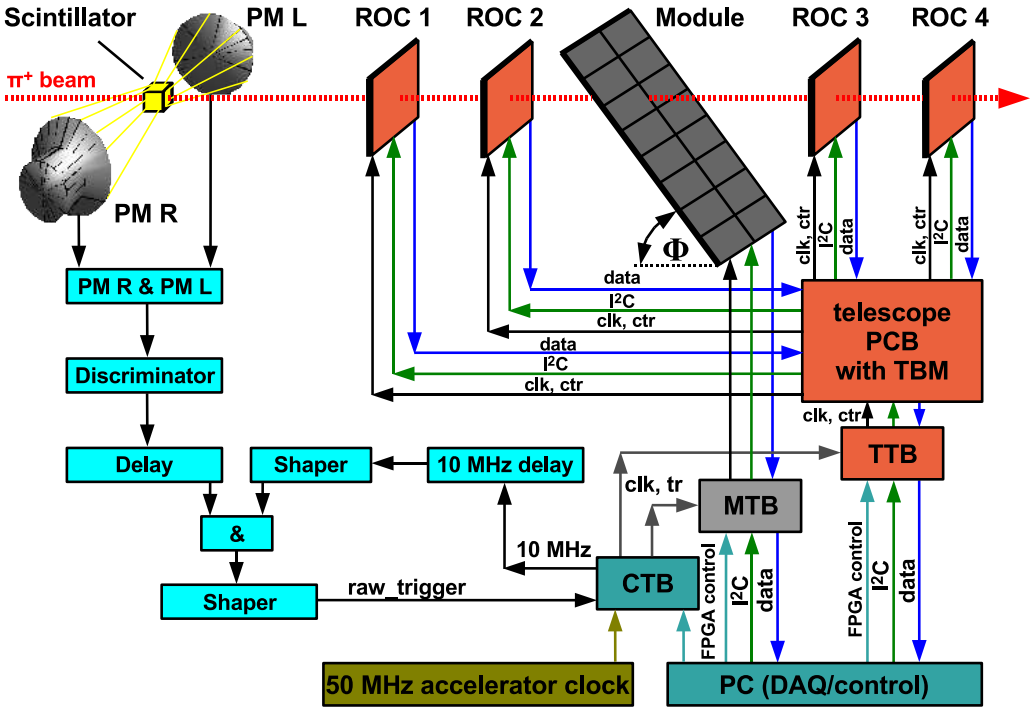

Figure 7.2: Schematic overview of the module beam test setup. It consists of the trigger part, the beam telescope with 4 single ROCs used for the track reconstruction and the module. For DAQ and controlling the setup a PC was used.

the 4 ROCs. The beam telescope was operated by the Telescope Testboard (TTB). The MTB and the TTB are testboards containing the same functions, since from the testboards point of view, the telescope and the module look identical with only one difference. The module has 16 ROCs and the telescope has only 4 ROCs. In total three standard multi purpose testboards were needed for the operation of the module beam test setup. Besides the TTB and the MTB a central Control Testboard (CTB) for running the setup was required. The schematic overview of the functionalities from the TTB, the MTB and the CTB is shown in Figure 7.4. The function of the CTB was especially adapted to the requirements for the operation of the module beam test.

For controlling the module/telescope the MTB/TTB is equipped with a FPGA. This device can be set up to route the externally applied clock frequency and the control signals for the operation directly to the module/telescope. These control signals are the “trigger” and the “reset” signal which are provided to the MTB/TTB together with the “clock” signal by the CTB. In addition the FPGAs contain a programmable local calibrate-trigger-reset generator (“CTR generator”). This generator can be used e.g. out of the beam time periods for the creation of the operating signals for investigations without beam. During the beam time periods additional calibrate pulses to the particle signals can be given by this “CTR generator” for special measurements. In the case of two simultaneous appearing trigger signals, one related to a particle and one from the local “CTR generator”, the internal one will be used and the particle trigger will be discarded. For every control signal (calibrate pulse, internal or

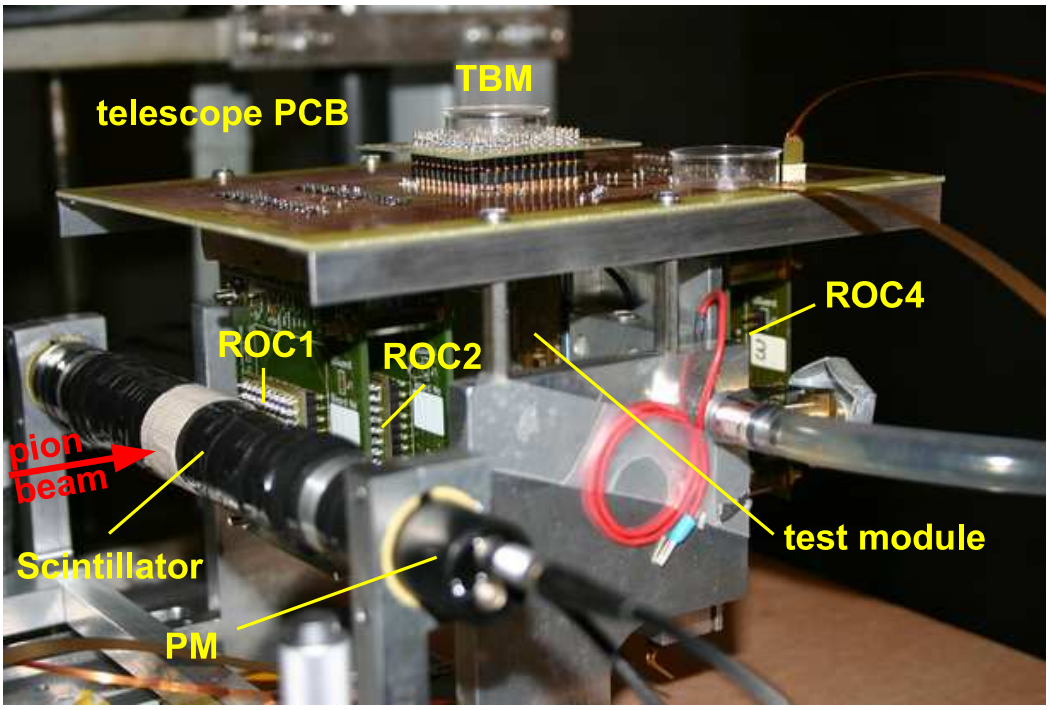

Figure 7.3: Setup used in the module beam test. On the left side one can see the tube in which the scintillator is located for trigger generation. At both front faces of the tube the PMs are attached. The module is mounted on the tiltable cooling block and located between the 4 ROCs of the beam telescope.

external trigger, reset) sent to the module/telescope the content of a special "event counter" is written to the 64 MByte memory on the testboard in combination with the type of the signal. Later on the data are transferred to the DAQ PC. Since the "event counters" on the MTB and the TTB are running synchronously and counting the clock cycles, the control signals have the same event number on both boards. For reading out the module/telescope the data stream from the module/telescope is digitized by a 12-bit Analog Digital Converter (ADC) on the MTB/TTB. To each event the content of the "event counter" is prefixed. The readout length of the module and the telescope is different due to the different number of ROCs. Therefore the readouts of the module and the telescope are running asynchronously. The assignment of the events from the telescope and the module occurs by counting the triggers and events. In addition the event number in the TBM header is used. The digitized data from the ADCs prefixed with the "event counter" contents, were written to the fast 64 MByte RAMs on the testboard. From there the data are transmitted via the USB[2] interface to the DAQ PC in the control room.

For the trigger generation the test setup was equipped with a plastic scintillator ($2 \times 2 \times 2$ mm^3) located in a tube made of furled Mylar®[3] foil. For the detection of the scintillation light photomultiplier tubes were attached to the Mylar tube on both front faces.

[2]USB = Universal Serial Bus

[3]Mylar is a polyester film and a registered trademark of DuPont.

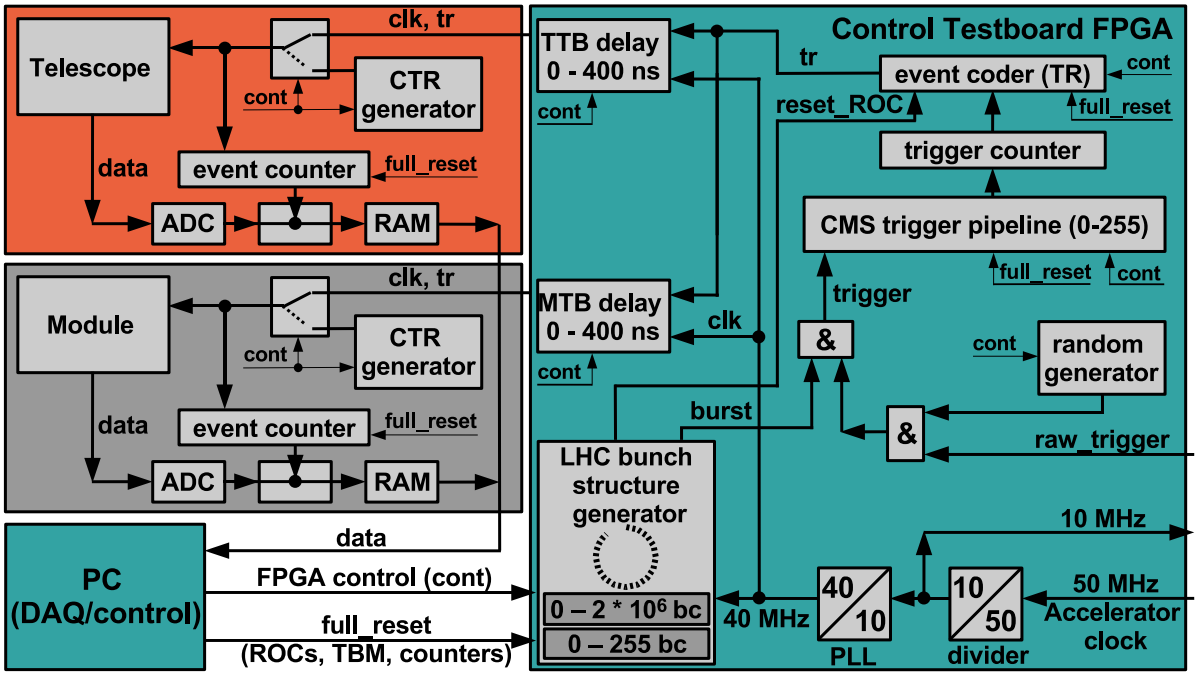

Figure 7.4: The control and readout system of the module beam test setup. The MTB and the TTB are identical. The CTB simulates the CMS environment for the beam test. The FPGA of the CTB contains the LHC bunch structure generator, the trigger pipeline, the event coder and the delays for shifting the setup versus the beam structure. The 10 MHz signal is used by NIM logic units to generate the "raw_trigger" signal (Fig. 7.2). In the text the signal and the functional blocks are given in quotation marks.

For processing the PM signals NIM[4] logic units (e.g. coincidences, discriminators, delays, shapers) were used.

The control testboard imitates the LHC and the CMS environment for the beam test of the module. In Figure 7.4 the schematic view of the FPGA on the CTB is shown. In principle, the testboard is in the case of the CTB used as a PCB carrier for the FPGA providing several possibilities for connections by dedicated daughter boards. The main functions of the CTB are to supply the MTB and the TTB with the 40 MHz system clock and to generate the trigger signal for the module and the telescope in a CMS like manner. In the FPGA of the CTB the 50 MHz clock from the accelerator is divided by 5 giving a 10 MHz signal. Subsequently a Phase Looked Loop (PLL) generates from this 10 MHz signal the 40 MHz system clock. The 40 MHz clock frequency is fed to the MTB delay and to the TTB delay. In addition the system clock is used by the "LHC bunch structure generator". This unit mimics the LHC orbit structure including the orbit gap. Therefore it has two programmable counters which define the length of the orbit and the length of the orbit gap in numbers of clock cycles. During the orbit gap the "burst" signal is low and if required a "reset_ROC" signal is supplied to the event coder in this time period. In CMS the orbit gap is about 3.2 µs long and during

[4]The Nuclear Instrumentation Module (NIM) standard defines mechanical and electrical specifications for electronics modules used in experimental particle and nuclear physics.

this period just empty bunches are passing the interaction region of the CMS experiment. Thus in the CMS trigger signal a time period of the length of the orbit gap without triggers will appear regularly. The 10 MHz signal is in phase with every fifth clock cycle of the 50 MHz accelerator clock and with every fourth clock cycle of the 40 MHz system clock respectively. Defined by this frequency ratio the minimal number of clock cycles between two consecutive triggers was 3 in contradiction to the CMS experiment where at least two clock cycles spacing are allowed. For trigger generation the 10 MHz pulses are brought with the signals from the PMs of the scintillation crystal in coincidence (Fig. 7.2). The various shaper and delay units are needed to ensure that the 10 MHz signal is the dominating signal for the timing of the trigger. Thus it is guarantied that every "raw_trigger" signal is caused by a particle belonging to a bunch which is in coincidence with the 40 MHz system clock. To reduce the total number of triggers to the desired L1T rate the "raw_triggers" are brought in coincidence with a "random generator". This "random generator" was scalable to let pass 0-100 % of the "raw_triggers". In addition the resulting triggers were gated with the "burst" signal from the "LHC bunch structure generator". After this gate the accepted "triggers" were fed to the imitation of the CMS trigger latency ("CMS trigger pipeline"). Afterward the trigger pulses were counted and passed to the "event coder", which generates the combined trigger reset ("tr") signal which is sent to the MTB delay and to the TTB delay. These two programmable delay stages were used to shift the 40 MHz system clock and the "tr" signal independently for the MTB and the TTB with respect to the 50 MHz accelerator frequency. Doing this the timing between the test setup and the bunch structure was optimized (Sect. 7.5). For completely randomly chosen events independent of the scintillator signal the trigger part of the CTB could be set up in a mode of using only the "random generator" pulses for triggering.

Programming the registers of the FPGAs ("FPGA control" and "cont" in Fig. 7.2 and Fig. 7.2) of the MTB, the TTB and the CTB before a data run, is done via the USB interface by the PC which is also used for the DAQ. To synchronize the "event counters" of the MTB and the TTB respectively and to delete the content of the "CMS trigger pipeline" and the "event coder" a "full_reset" signal was sent at the beginning of each data run. The loading of all settings for the initialization of the registers in the ROCs of the telescope and the module is done directly by the PC via the USB interface using the adapted I^2C protocol ("I^2C" in Fig. 7.2 and Sect. 3.4).

7.3 Readout Data Losses of the Module

Due to the limited space available on the ROC the possibilities for the design of the readout architecture of the module and the ROC were restricted. To keep the data losses causing inefficiency as low as possible the readout scheme was carefully optimized by simulation studies. The readout of the ROC occurs in two stages. The first stage, called the "drain", takes place in parallel within each DCOL. During the column drain mechanism the address and the pulse height is copied from the pixels with a hit as fast as possible to the data buffers in the periphery of the DCOL (details in Sect. 4.1.2). In the second stage, called "readout", the triggered data is transferred from the DCOL periphery to the data acquisition system (Sect. 3.4). Also in the optimized readout architecture, there are still data losses present in both stages of the readout which will be discussed in the following sections.

7.3.1 Column Drain Data Losses

The DCOL data losses depend on the DCOL hit rate and the average number of pixels with a signal per DCOL. Therefore they depend on the pixel occupancy, which is related to the luminosity and the position in the detector. For high luminosity the averaged DCOL hit rate at 4 cm is about 1.4 MHz and on the average 2.2 pixels have a hit in a DCOL [21]. The "drain" losses do not depend on the L1T rate. The contributions to the "drain" losses are:

- Time stamp buffer overflow: The hits in a bunch crossing notify the DCOL periphery to set a time stamp. Therefore the 8-bits of the bunch crossing counter are stored in one of the 12 time stamp buffer cells. The time stamps must be stored for the duration of the L1T latency. If the event is not confirmed by a trigger, the corresponding time stamp is deleted. If, at any given time, this buffer happens to be full, the next time stamp will be lost, since data acquisition is paused until the next buffer cell is freed. The occupancy of the time stamp buffers depends on the DCOL hit rate and the L1T latency.

- Pixel busy: After the DCOL periphery is notified to set a time stamp the pixels with a hit wait for the column drain. The column drain is started after 2 clock cycles and the copying of the data to the periphery needs two clock cycles per pixel hit. On average about 6 cycles are needed to drain a DCOL. If the same pixel is hit again before its data is transferred to the periphery the additional hit will be lost. This data loss depends on the pixel occupancy and the speed of the column drain architecture.

- Column drain busy: On average 6 cycles are needed for the column drain. If the same DCOL is hit again during the running column drain the new hit can be queued. The queuing depth is limited to 3 hits. Any next DCOL hit will be lost. This loss depends on the DCOL hit rate and the column drain speed.

- Data buffer overflow: The 9-bit pixel address and the analog pulse height are stored in the data buffer to await the L1T latency. The data buffer has a depth of 32 units. If the total number of pixels stored from all time stamps is too large the DCOL is reseted and the content of the data buffer is erased. This loss depends on the pixel occupancy and the L1T latency.

In the upper part of the Table 7.1 the quantitative contributions of the "drain" losses are shown for the different radii of the pixel detector layers. The simulations were done for the high luminosity of 10^{34} $cm^{-2}s^{-1}$ and a L1T rate of 100 kHz [70]. For the 4 cm layer the different contributions of the "drain" losses are nearly equal and sum up to a total amount of about 0.80 %.

7.3.2 DCOL Readout Data Losses

The "readout" losses include data losses which occur when trigger confirmed pixel hits are read out from the ROC and the module respectively. These losses depend on the L1T rate and the average length of the data packets. The "readout" losses are composed of:

Radius [cm]	4	7	10
Time stamp buffer overflow	0.17 %	0.001 %	0
Pixel busy	0.21 %	0.078 %	0.044 %
Column drain busy	0.25 %	0.020 %	0.004 %
Data buffer overflow	0.17 %	0.081 %	0.065 %
1-Buffer	1.0 %	0.40 %	0.26 %
Double column block	1.0 %	0.20 %	0.16 %
Double column reset	1.0 %	0.44 %	0.26 %
total	3.8 %	1.2 %	0.79 %

Table 7.1: Summary of the simulated data losses for the pixel detector at high luminosity operation (10^{34} cm^{-2}s^{-1}) and 100 kHz L1T rate. The upper part shows the column drain losses and in the lower part the readout related data losses are summarized.

- 1-Buffer: Per DCOL only one L1T confirmed event can be processed. If a second time stamp is confirmed by a L1T during the DCOL is awaiting for the readout of the first confirmed event, the second L1T will be lost.
- Double column block: After a time stamp in a DCOL has been confirmed by the L1T the DCOL's drain mechanism is blocked. No farther pixels can be stored until the DCOL is fully read out.
- Double column reset: After an event is read out the DCOL resets itself and any stored data are erased in the data and time stamp buffers.
- TBM stack overflow: The TBM chip transmits the L1T signal to the ROCs and initiates the readout by sending the token signal out. If a L1T signal arrives while a readout is in progress on the module it has to be queued on the event stack in the TBM. If the 32-deep stack becomes half full the next L1T will not be forwarded to the ROCs. The TBM will send in this case just a header followed by a trailer. According to the simulations this loss is negligible.

The contributions of the "readout" losses are summarized in the lower part of the Table 7.1. For the 4 cm layer the "readout" losses sum up to about 3.0 % and in total data losses of 3.8 % were expected according to the simulations for high luminosity. For the 7 cm and 10 cm layer the total data losses are 1.2 % respectively 0.79 %. Hence the "readout" losses are the dominating data losses for high luminosity operation and a L1T rate of 100 kHz for all three layers.

7.4 Comparison of the Beam Test with CMS

The goal of the beam test was to operate the module under LHC like conditions. According to the simulations done with the algorithm used for the data loss calculations (Sect. 7.3) these conditions mean e.g. for the innermost layer of the pixel detector a track density of 26 MHz/cm^2 [21]. This fluence is averaged over the covered η range and corresponds to

40 MHz/cm^2 for $\eta = 0$. With an expected pixel multiplicity of about 5.5 in the 4 T magnetic field causing charge sharing between pixels this track density results in a pixel fluence of about 143 MHz/cm^2. Furthermore in CMS not for every L1T signal a track will occur in a defined region of a module. In the beam test no magnetic field was applied and therefore the measured pixel multiplicity was in the range of 1.1. Additionally every trigger signal is caused by a particle passing the scintillator. If the tracks of these particles could be reconstructed with the 4 ROCs of the telescope they have traversed the module in the region of the scintillator shadow. The CMS track density of 26 MHz/cm^2 would result in a pixel fluence of about 29 MHz/cm^2 in the beam test and the CMS pixel fluence of 143 MHz/cm^2 would be related to a track density of 130 MHz/cm^2 in the beam test with a pixel multiplicity of 1.1. Therefore the track density from the beam test could be compared neither with the track density nor with the pixel fluence of the CMS simulation. Since in CMS the pixel hits are correlated expressed by the pixel multiplicity of 5.5 compared to 1.1 from the beam test. Because of this fact the DCOL trigger rate was chosen as parameter for the comparison. The DCOL trigger rate is the number of tracks traversing a DCOL and causing a trigger signal. This number is independent of the pixel multiplicity.

In the beam test the scintillator shadow covered about 10 double columns on ROC 3 and ROC 12 (see Fig. 7.9) on the module. Thus the adjusted trigger rate divided by 20 gives the DCOL trigger rate. This number has to be compared with the CMS DCOL hit rate divided by the bunch structure of 40 MHz and multiplied with the L1T rate of 100 kHz. For the comparison of the beam test results with the simulated data losses the simulation was adapted to the beam test conditions. Therefore only particles in a region of 10 DCOLs could cause a trigger. In addition the L1T rate which is an input parameter for the simulation was adapted for every fluence value to achieve the DCOL trigger rate of the beam test. The trigger rate was kept constant for a fluence scan. In Figure 7.5 the data losses are shown in dependence of the fluence for barrel modules with a trigger rate of 20 kHz. The data losses are calculated with the adapted simulation algorithm. For low intensities the "readout" losses, which are related to the L1T rate, are the significant contribution to the total data losses. For high track densities the "drain" losses which depends on the L1T latency and the DCOL hit rate are dominant. For comparison of the beam test results and the beam test simulations with the CMS simulation one has to estimate the fluences related to the DCOL hit rates. The averaged DCOL hit rate e.g. of the 4 cm layer is 1.4 MHz in CMS. Due to the pixel multiplicity of about 1.1 this number multiplied by the number of DCOLs per ROC and divided by the sensitive area of the ROC gives the corresponding fluence for the beam test which is about 62 MHz/cm^2. The averaged DCOL hit rates for the 7 cm and 10 cm layer are 0.62 MHz respectively 0.36 MHz. The appropriate fluences are about 28 MHz/cm^2 and 16 MHz/cm^2. In Figure 7.6 the DCOL trigger rates are shown for CMS conditions with a fixed L1T rate of 100 kHz and for the trigger rates of the beam test. The CMS DCOL trigger rate scales with the intensity. For the beam test the trigger rates were kept constant.

The approach was to reproduce the beam test inefficiencies with a dedicated simulation to prove that the data loss mechanisms are understood. In this case the simulated data losses for CMS (Table 7.1) are confirmed.

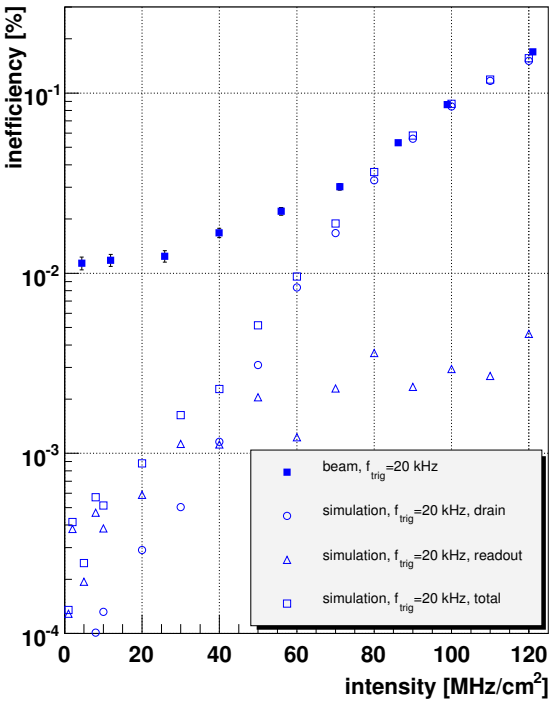

Figure 7.5: Simulated data losses for beam test conditions with a trigger rate of 20 kHz. For low intensities the "readout" losses and for high fluences the "drain" losses are dominating the total data loss.

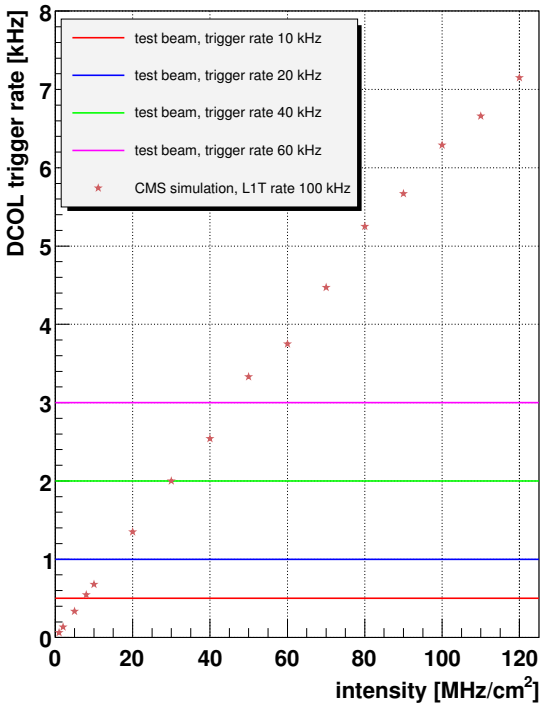

Figure 7.6: The DCOL trigger rates for CMS scales with the fluence. In the beam test the trigger rate was kept constant.

7.5 Commissioning of the Beam Test Setup

During the commissioning phase of the beam test setup fine adjustments concerning the latency of the module and the phase of the system clock with respect to the accelerator frequency were done.

7.5.1 Latency Scan with the Module

The control testboard contains a trigger pipeline which delays the trigger pulses by a programmable number of cycles. This introduced delay represents in the module beam test the time needed for the level-1 trigger decision in CMS. During the trigger latency the ROC has to store all data locally. To find out in which bunch crossing the particle passed the module, which caused a trigger, a latency scan with the module was performed. The scans took place at a low particle track density and at a low trigger rate. For the measurements the programmable difference between the bunch crossing counter (WBC) and the Second Bunch crossing Counter (SBC) in the double column periphery of the module ROCs were varied (Sect. 4.1.2). The counted number of triggers divided by the number of not empty readouts

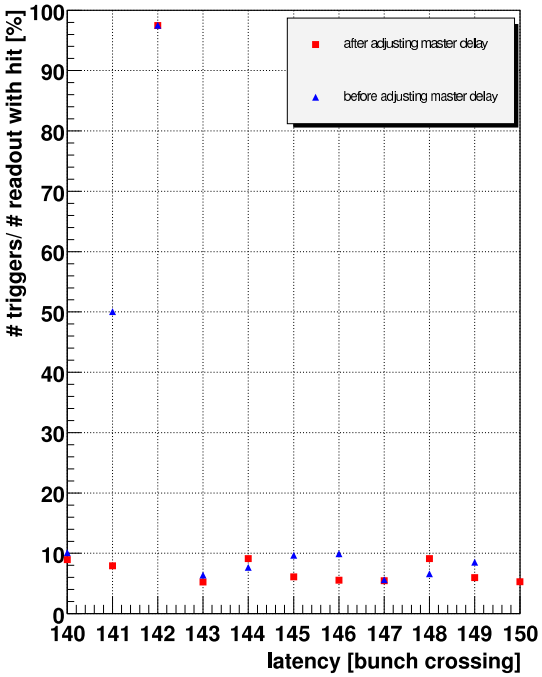

Figure 7.7: After the fine adjustment of the 40 MHz system clock regarding the 50 MHz bunch structure about 99 % of the triggered readouts had a hit for a latency of 142 bunch crossings.

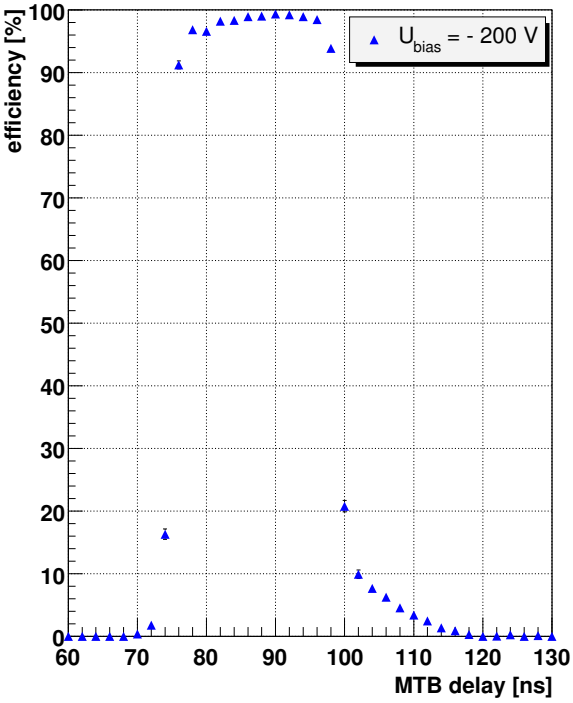

Figure 7.8: For the optimization of the phase between the 40 MHz system clock and the 50 MHz accelerator frequency a delay scan with the MTB delay was performed. A plateau with a length of about 22 ns with a high efficiency was observed.

versus the programmed latency is shown in Figure 7.7. For comparison the measurements were performed before and after the fine adjustment between the system clock and the accelerator frequency (Sect. 7.5.2). According to the latency scan the particles causing trigger signals have been 142 bunch crossings ahead. Therefore the default trigger latency was set to 142 for the entire beam test period despite the fact that the CMS latency will probably be 128 bunch crossings.

7.5.2 Delay Scan with the Module

To optimize the phase of the 40 MHz system clock with respect to the 50 MHz accelerator frequency a delay scan with the MTB delay (Fig. 7.4) was performed. The scan was done at a low track density and at a low trigger rate. The result is shown in Figure 7.8, where the efficiency versus the delay in nanoseconds is plotted. The plateau length is in the range of 22 ns which is consistent with the periodic time of the system clock. After the scan the MTB delay was adjusted to 88 ns in the middle of the plateau for the beam test period. For more details concerning the delay curves and various dependencies of the delay curves see

Section 7.6.6.

7.6 Measurements and Results

It was the first time that 16 ROCs and a TBM were operated together in high rate beam. The ROCs and the TBM cooperated very well under LHC like conditions.

The most interesting investigations were the inefficiency measurements. These measurements can be performed under realistic conditions only in a high rate beam. Therefore most of the beam time was used for measuring the efficiency in dependence of e.g. the track density, the trigger rate, the latency and the threshold. Furthermore crosstalk investigations and measurements with the tilted module were done. All measurements were performed with a latency of 142 bunch crossings besides the investigations of the inefficiency as a function of the latency (Sect. 7.6.3). Exemplary a module hit map is shown in Figure 7.9. This hit map is a superposition obtained by continuous data taking and simultaneous readout operation over 6 seconds with a comparator threshold of 2900 electrons and a trigger rate of 10 kHz. The fluence was about 120 MHz/cm^2 in the region of the telescope. The intensity of the beam was not completely homogeneously over the entire module in the beam test. The rows and columns with more hits are the edge pixels of the ROCs since they are connected to sensor pixels with an increased size (Sect. 3.1.5). The scintillator shadow covers 10 DCOLs on ROC 3 and ROC 12.

7.6.1 Inefficiency for different Trigger Rates

The inefficiencies for various track densities and different trigger rates are shown in Figure 7.10. The measurements of the complete fluence scans were performed with trigger rates of 10 kHz and 20 kHz. At fluences of 40 MHz/cm^2 and 100 MHz/cm^2 the inefficiencies were measured for 40 kHz and 60 kHz trigger rates additionally. The trigger pulses were given by the scintillator and scaled down by the random generator implemented in the FPGA on the CTB (Sect. 7.2). With the CTR generator on the MTB the intensity scan labeled as "calinj" was done. In this operation mode of the MTB, the calibrate pulses and the corresponding triggers had priority compared to the triggers related to the beam particles. The beam is used for generating stochastic data traffic on the module. The efficiency in this mode is determined by checking if the test-pixel which got the calibrate injection is also present in the read out event. If not, one of the sources for data loss prevented the appearing of the test-pixel hit (Sect. 7.3). The measurements with beam or calibrate pulses were performed with a global threshold of about 2900 electrons.

For comparison with the measurements the expected inefficiencies according to the adapted simulation are plotted. For an intensity of 62 MHz/cm^2 corresponding to the innermost layer of the pixel detector the measured inefficiency is about 2 % in contrast to the expected one of 1 %. In principle the measured inefficiencies are consistent with the results from the simulations for fluences higher than 80 MHz/cm^2. For lower track densities the measurements show an inefficiency higher than predicted by the simulations. Especially the inefficiencies were always higher than about 1 %. Concerning the "calinj" measurements the simulated inefficiencies were confirmed for fluences higher than 60 MHz/cm^2 where the "drain" losses

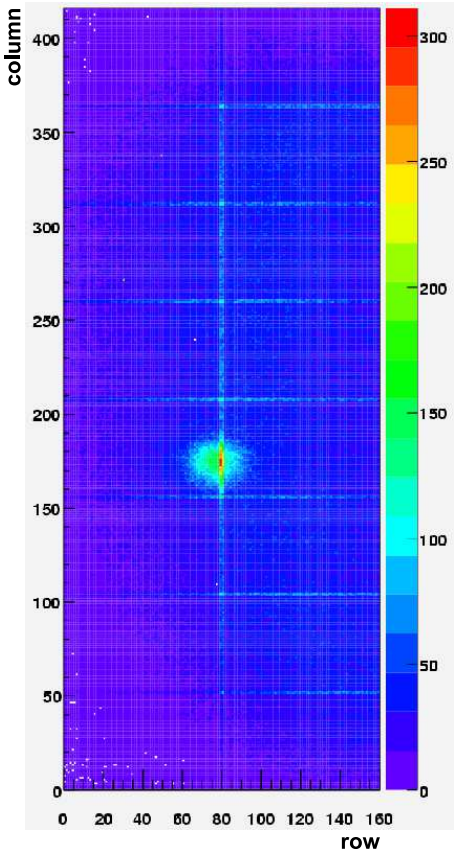

Figure 7.9: Module hit map achieved with a beam intensity of about 120 MHz/cm^2 and a comparator threshold of 2900 electrons. The number of hits per pixel show the right hand bar.

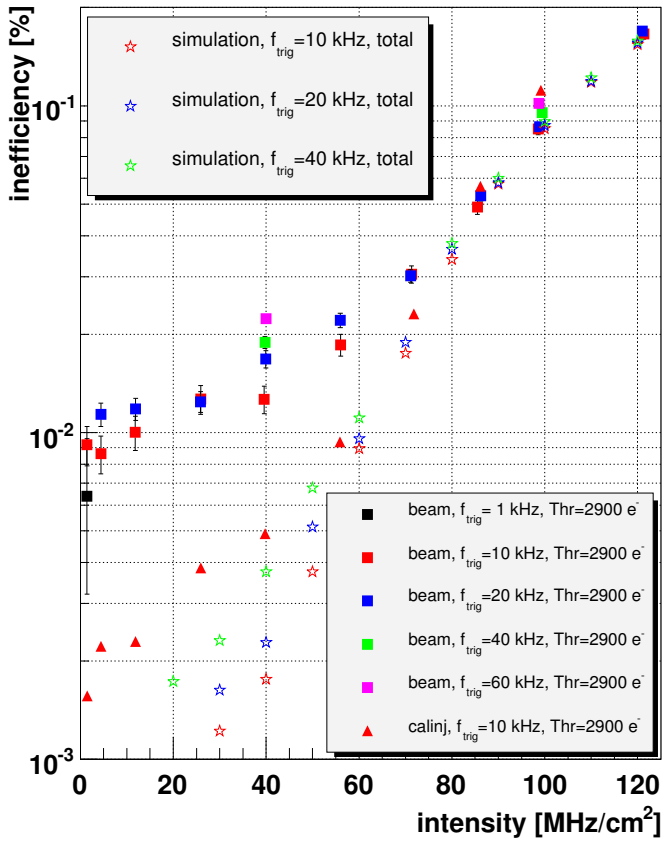

Figure 7.10: The inefficiencies versus the track densities for different trigger rates measured in the beam test. The corresponding results from the simulations and the measurements with additional calibrate signals are also shown.

are dominant. For lower fluences the measured inefficiencies are higher than simulated but lower than measured with the beam. Since there were only triggers found related to the calibrate pulses and no triggers for beam particles in the "calinj" data files, the "readout" losses dominant for low fluences are not taken into account correctly in this measurement. However, the expected "readout" losses are not as large as needed to explain the discrepancy between the "calinj" and the beam measurements. The "readout" losses are only in the per mil range (Fig. 7.5).

The dominant contribution to the inefficiencies for high fluences are the "drain" data losses (Sect. 7.3.1 and Fig. 7.5). These data losses are independent of the L1T rate and therefore the simulated inefficiencies are equal for high intensities and different trigger rates. At low intensities the "readout" part of the data losses, which depends on the L1T rate, is dominant. Thus the simulated inefficiencies are higher for higher L1T rates. The measured inefficiencies

show in principle the expected behavior. At 40 MHz/cm^2 the inefficiencies are increasing with the L1T rate. At 100 MHz/cm^2 the inefficiencies still increase with the L1T rate which was not expected since in this fluence region the contributions of the "drain" losses are dominant (Sect. 7.5).

A possible explanation for a part of this discrepancy for lower fluences may be the sensor inefficiency. This data loss is not taken into account in the simulation and in the measurements with the calibrate pulses. According to the pixel sensor studies (Sect. 3.2.3.1) [32] the fraction of lost hits for a comparator threshold of about 3000 electrons depends on the irradiation of the sensor. Since no total fluence determination was done during the beam test, the irradiation fluence was estimated with equation (Sect. 4.2.1):

$$\frac{\Delta I}{V}\frac{1}{\alpha} = \Phi \tag{7.1}$$

The change ΔI at total depletion is normalized to the sensitive volume V of the sensor. The variation of the current with fluence Φ is expressed in terms of the damage rate α ($\alpha = 3.99 \times 10^{17}$ A/cm [92]). With the measured leakage currents during the beam test normalized to a temperature of 20 ℃ using the temperature dependence of the volume generation current ($I \propto T^2 \exp\left(-\frac{E_{gap}}{2k_B T}\right)$) the absorbed irradiation fluence for the entire beam test period of about 8 weeks was estimated to be in the range of 0.5×10^{14} n_{eq}/cm^2. The scaling factor for pions with a momentum of 300 MeV/c compared to 1 MeV neutrons is 0.94. Therefore the measured sensor inefficiency for this irradiation fluence is about 0.5 %.

Another source of data loss which is not taken into account in the simulation results from the fact that the DCOL trigger rate in the scintillator shadow on the module is not uniform. This may be caused by the divergence of the beam and means that some DCOLs have a higher DCOL trigger rate. This is responsible for higher "readout" losses. The measured contribution to the inefficiency is in the range of 0.2 % [93].

7.6.2 Inefficiency for different Comparator Thresholds

With the trimming mechanism described in Section 7.1 trim maps for different global thresholds have been generated. The used global thresholds were 1925, 2250, 2900 and 4200 electrons. The inefficiencies depending on the track densities for different global thresholds and a trigger rate of 10 kHz are shown in Figure 7.12. For comparison the simulated data losses are also plotted.

For all available trim maps the measured inefficiencies are higher than expected according to the simulations for low fluences. The higher inefficiencies for a global threshold of 4200 electrons for low track densities may be caused by the fact that the trimming mechanism uses the absolute comparator threshold. But the time between a particle crossing the sensor and the comparator going above the threshold depends on the created ionization charge. Therefore it might happen that for low pulses the signal is delayed to the next bunch crossing and hence is lost during trigger validation. In Ref. [70] this time walk behavior is described in detail. According to these investigations for an absolute threshold of 4200 electrons the usable threshold (in-time threshold) may be about 5000 electrons. That means that the time difference between a signal of 5000 electrons and very high charges above 100 ke$^-$ is below 25 ns. In principle a higher threshold cuts the Landau pulse height spectra (Sect. 3.2.1) and

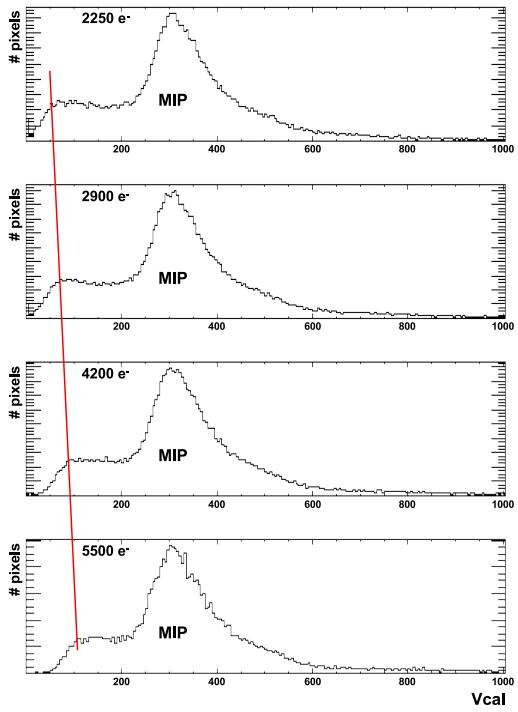

Figure 7.11: Pulse height spectra for different global comparator thresholds. The thresholds in electrons are the absolute comparator thresholds.

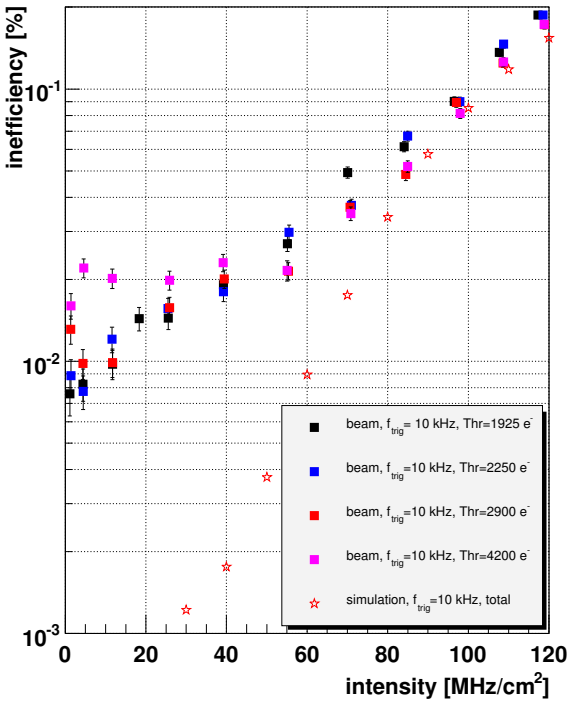

Figure 7.12: Inefficiency versus the track density for different global comparator thresholds and a trigger rate of 10 kHz.

may be responsible for the additional inefficiency. Different pulse height spectra for various global thresholds can be seen in Figure 7.11.

7.6.3 Inefficiency for different L1T Latencies

In Figure 7.13 the measured inefficiencies versus the fluences for 3 different latencies (122 bunch crossings (bcs), 142 bcs and 162 bcs) and a constant trigger rate of 10 kHz are shown. The "drain" losses depend on the L1T latency (Sect. 7.3.1). The expected higher data losses for higher latencies can be seen. The effect of the higher latency increases with the fluence since with the intensity also the dominance of the "drain" losses are increasing (Fig. 7.5). At a fluence of 100 MHz/cm^2 the inefficiencies for latencies of 102 bcs, 82 bcs and 70 bcs were measured additionally.

In Figure 7.14 the measured and simulated inefficiencies at a constant fluence of 100 MHz/cm^2 with a trigger rate of 10 kHz are shown. Overall the inefficiency decreased with shorter L1T latency. The inefficiency of 8.5 % at latency of 142 bcs was reduced to about 6 % at a latency of 128 bcs. The CMS latency will be 128 bunch crossings and the beam test was performed at a latency of 142 bcs. The discrepancy for low latencies between the measured and the simulated data losses is not really understood but may be related to

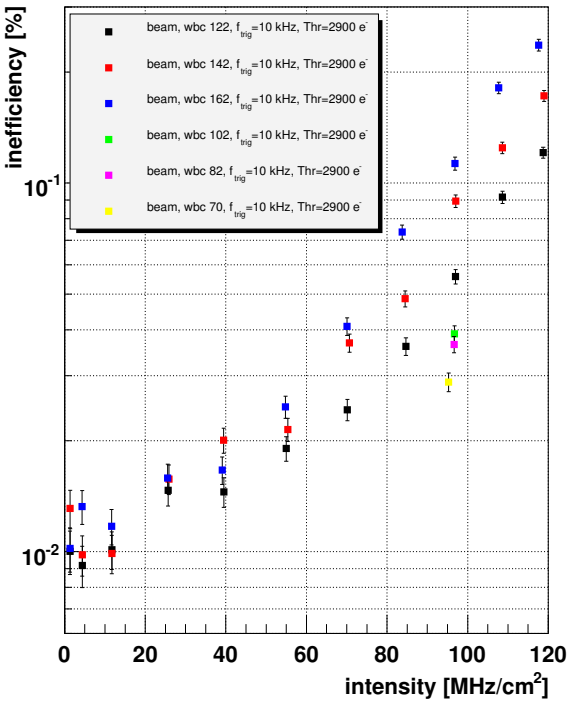

Figure 7.13: The inefficiencies for latencies of 162 bunch crossings, 142 bcs and 122 bcs measured at the beam test. The dominance of the "drain" losses is increasing with the fluence.

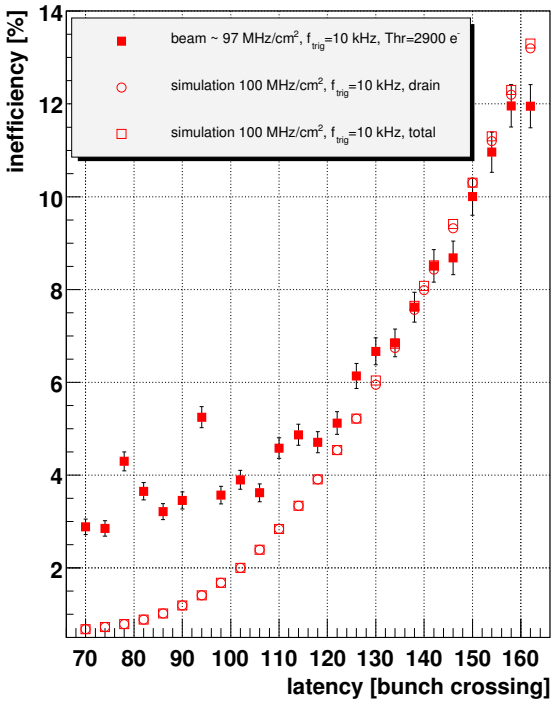

Figure 7.14: The measured and simulated inefficiencies for different latencies at a fluence of 100 MHz/cm^2. The CMS latency is 128 bunch crossings and the beam test was performed at a latency of 142 bcs. The difference in the efficiency is at a fluence of 100 MHz/cm^2 in the range of 2 %.

the higher inefficiencies for low track densities as described in the Section 7.6.1.

7.6.4 Crosstalk induced Threshold Shift

The crosstalk on the module was investigated in detail in the laboratory and the results are described in Chapter 6. The conclusions of the laboratory measurements were that the crosstalk is negligible under real conditions. To crosscheck this results s-curves were measured for a single pixel without beam and with a fluence of 40 MHz/cm^2 and 100 MHz/cm^2. To perform this measurements the local CTR generator on the MTB was used to generate calibrate pulses and triggers which had priority compared to the triggers related to the beam particles. The beam caused stochastic data traffic on the module and the height of the calibrate pulses was varied. The achieved s-curves are shown in Figure 7.15.

Without beam particles the width of the s-curve is about 2 V_{cal} DAC values which corresponds to 130 electrons. With 100 MHz/cm^2 beam fluence the width is in the range of 225 e$^-$ and the relative threshold shift was about 300 electrons compared to the case without the

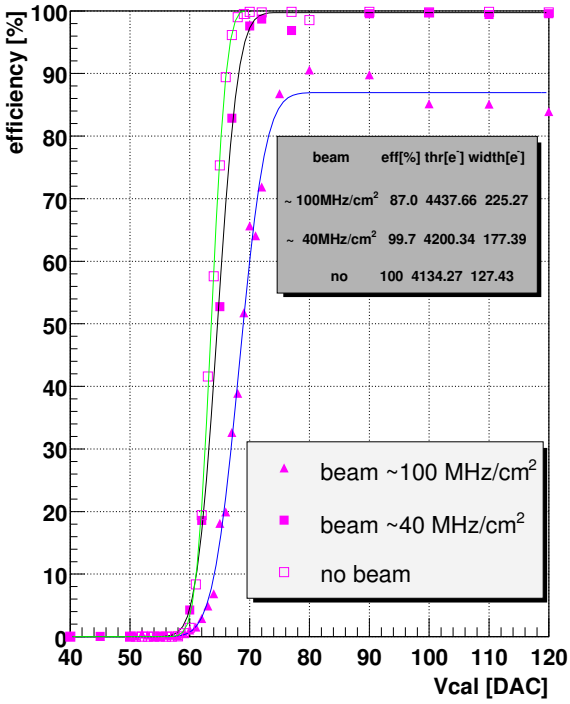

Figure 7.15: S-curves measured without beam and for fluences of 40 MHz/cm^2 and 100 MHz/cm^2. The relative threshold shift is in the range of 300 e$^-$ and the width increased from 130 e$^-$ to 225 e$^-$.

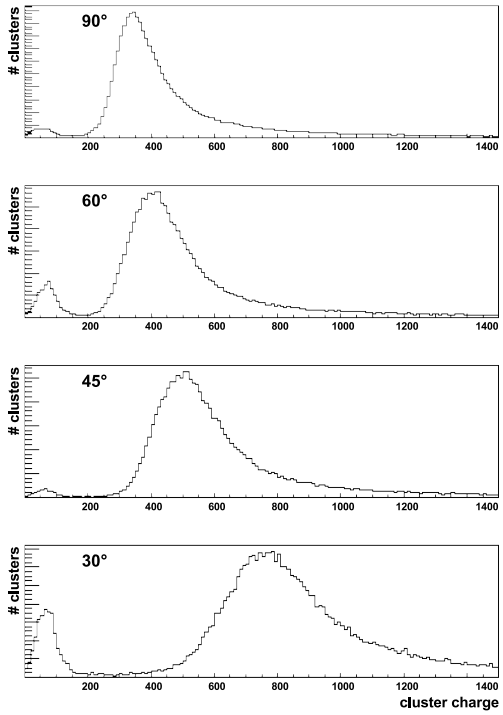

Figure 7.16: The cluster charge increases with the thickness of the sensor divided by the sine of the angle between the beam and the module ($Q_{cluster} \propto t/\sin\Phi$). The cluster charges for 30°, 45°, 60° and 90°.

beam. These results are consistent with the laboratory measurements, where the threshold shift was about 200 e$^-$ for realistic cluster sizes. The threshold shift and the increased noise is negligible compared to the planned global comparator threshold of 2500 electrons.

7.6.5 Cluster Charge for various Angles

For different angles Φ between the incident beam and the module surface the reconstructed cluster charge is shown Figure 7.16. The hit maps for the measured angles of 0°, 30°, 45°, 60° and 90° are shown in Figure 7.17. 90° means that the beam was perpendicular to the module surface and for 0° the beam was parallel to the module. The single pixel charge decreases with Φ and the cluster charge increases with the thickness of the sensor divided by the $\sin\Phi$. This tendency can be seen in the plots of the cluster charges. The second peak in the cluster charge plots at small charges may be caused by "delta rays". δ-electrons are emitted from atoms by the passage of charged particles through matter. Any charged particle traversing a medium transfers energy to that medium via the process of ionization or excitation of the constituent atoms. Due to the statistical fluctuations in energy loss, there is some probability of transmitting energy in excess of a few keV. δ-electrons have enough

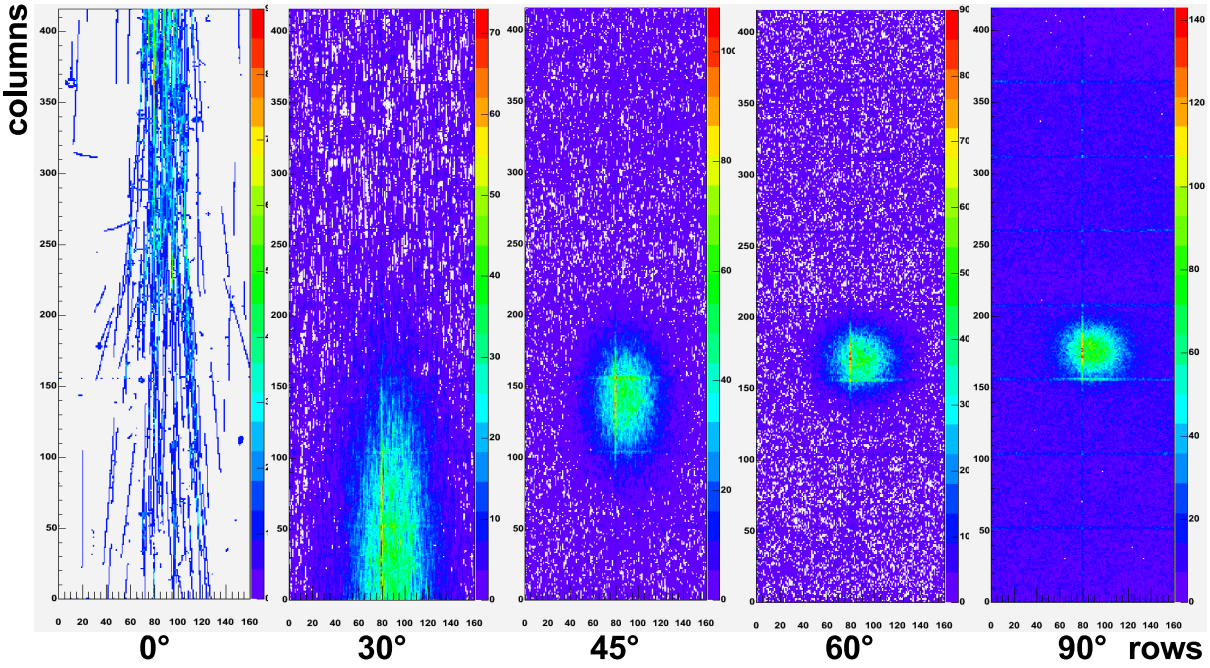

Figure 7.17: Module hit maps for different angles between incident beam and module. Red (violet) corresponds to a high (low) number of hits.

energy to produce, themselves, fresh ions in traversing the medium (secondary ionization) and create detectable tracks. Some examples of these tracks, nearly perpendicular to the main beam direction, can be seen in the hit map for 0°. The corresponding cluster charges could be responsible for the second peaks in cluster charge plots. According to this attempt of explanation it is not clear why these second peaks are not present for 45° and 90°.

7.6.6 Delay Scans for different Comparator Thresholds and Bias Voltages

The delay defines the phase of the system clock with respect to the accelerator frequency. The goal of the delay scans was to find for different parameters as the global comparator threshold and the bias voltage for the sensor a common range of delays where the modules can be operated properly. This will be important for the pixel detector since e.g. the V_{bias} has to be adapted with the ongoing irradiation of the sensors during operation.

In Figure 7.18 the inefficiency versus the delay for different global thresholds is shown. The time difference between a particle crossing the sensor and the comparator going above the threshold depends on the created ionization charge and the comparator threshold. Therefore the 25 ns delay window with low inefficiency appears shifted in time for various thresholds. In principle the plot represents the time walk behavior of the module (Sect. 7.6.2).

The dependence of the delay on the bias voltage can be seen in Figure 7.19. For a higher V_{bias} the charge collection occurs faster in the sensor ($\vec{v} = \mu \cdot \vec{E}$ with μ is the mobility) and therefore the window with high efficiency appears earlier. In addition the V_{bias} has an impact

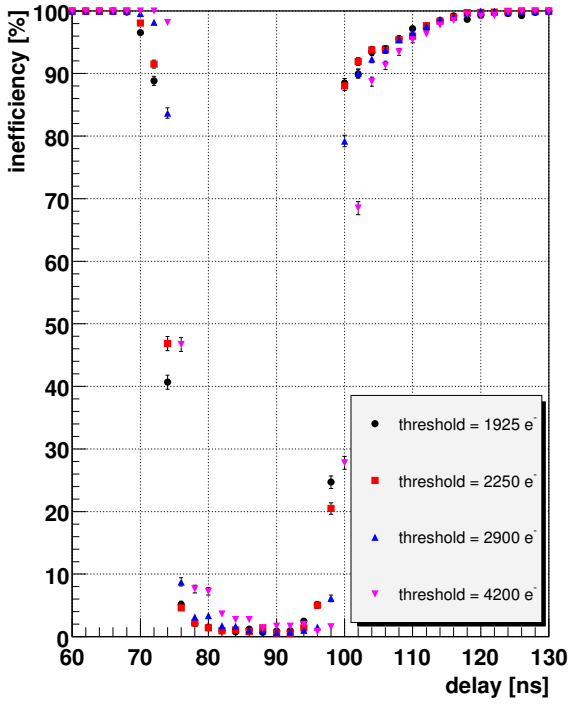

Figure 7.18: Delay scans for different global comparator thresholds. The correct time window for high efficiency is shifted in time with the different thresholds.

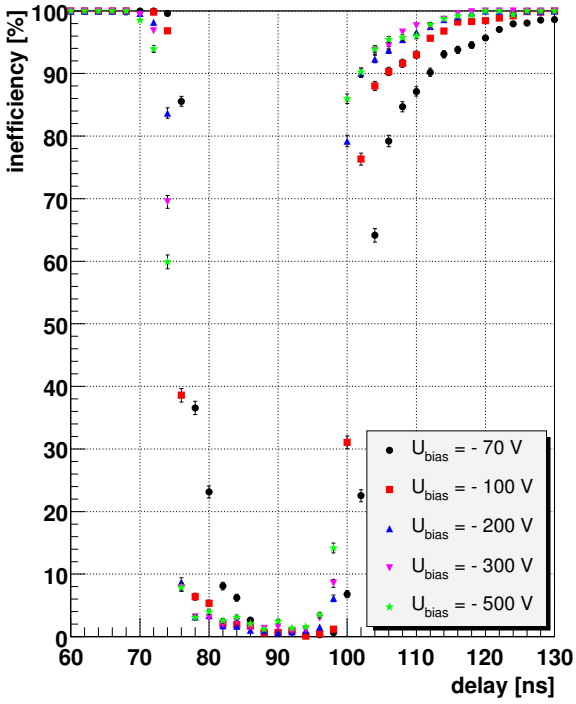

Figure 7.19: Delay scans for different bias voltages. The correct time window for high efficiency is shifted in time with the different V_{bias}.

on the collected charge versus the time and thus on the pulse shape. This results in a steeper slope and a broader plateau for the optimal time window for a high V_{bias} and vice versa. The adjusted delay for the beam test was 88 ns which is conform with several global thresholds and bias voltages.

7.6.7 TBM Readout Stack

The stack of the TBM contributes to the "readout" losses (Sect. 7.3.2) of the module. According to the simulations these contributions are negligible. In Figure 7.20 the time in numbers of bunch crossings (bcs) between a trigger and the corresponding readout is shown for a run with a fluence of 10 MHz/cm^2 and a trigger rate of 24 kHz. Most of the readouts starts with a delay of 28 bcs after the trigger pulse. This delay is related to the beam test setup and means that the readout is started immediately after the trigger signal. However some triggers have to be queued in the TBM stack. These triggers cause the flat region in the left plot of the Figure.

In addition the time between consecutive triggers is shown. Since it is a logarithmic plot for the random triggers a linear decrease is expected and confirmed by the measurement.

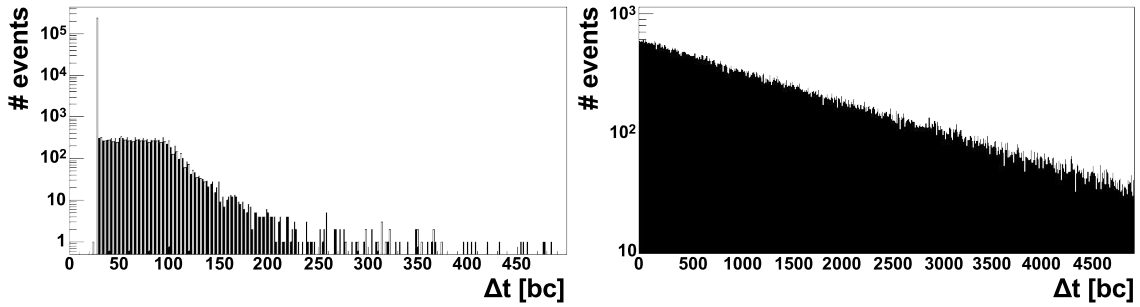

Figure 7.20: The time difference between the trigger and the start of the readout operation in clock units (left plot). The time difference between randomly chosen triggers (right plot).

7.7 Interpretation of the Results

The intention of the beam test was to operate a final module under LHC like conditions. No operational problem in the interaction of the 16 ROCs with the TBM was observed under these conditions. In Section 7.4 the difficulties are described how to find a parameter which is adequate to compare the results of CMS simulations with the results from the beam test. The main reason for the differences are the global L1T rate in CMS and the locally given trigger rate by a scintillator in the beam test. Hence the track density and the pixel fluence is not useful for a comparison since the 5 times higher pixel multiplicity in CMS and the resulting correlation of the hits is not realistic for the beam test without a magnetic field. The chosen parameter was therefore the DCOL trigger rate. The further approach was to adapt the data loss simulation algorithm to the beam test conditions with a fixed DCOL trigger rate for various fluences. The simulated inefficiencies confirmed the measured data losses from the beam test for high track densities above 80 MHz/cm^2 but not for fluences below this value (Fig. 7.10). Regarding the latency scan (Fig. 7.14) the simulation is consistent with the measurements only for latencies higher than 130 bunch crossings. Both discrepancies from the fluence scan and the latency scan could be explained with an underestimation of the "readout" data losses. This data loss part depends on the L1T rate and it dominates the sum of data losses for low fluences (Fig. 7.5). Looking on the DCOL trigger rates of the DCOLs covered by the scintillator it was realized that these rates are not uniform due to the divergence of the beam. This fact causes higher "readout" losses in some DCOLs and is responsible for an additional inefficiency of 0.2 %. The "drain" losses seem to be correctly taken into account, since the "calinj" measurement in Figure 7.10 follows the simulation with only a small discrepancy in the per mill range for low fluences. In addition there may be a sensor inefficiency of about 0.5 % caused by the collected irradiation of the sensor. This inefficiencies are not included in the simulation and the "calinj" measurement. In Figure 7.21 the simulated inefficiencies and the "calinj" inefficiencies are shown corrected with an additional data loss of 0.7 %.

The most important issue is not the absolute measured inefficiency but the question if the data losses are described correctly in the simulation. After all it seems to be reasonable that the measured inefficiencies in the beam test could be reproduced by the simulations. This means that the data losses are taken into account correctly in the simulation and therefore

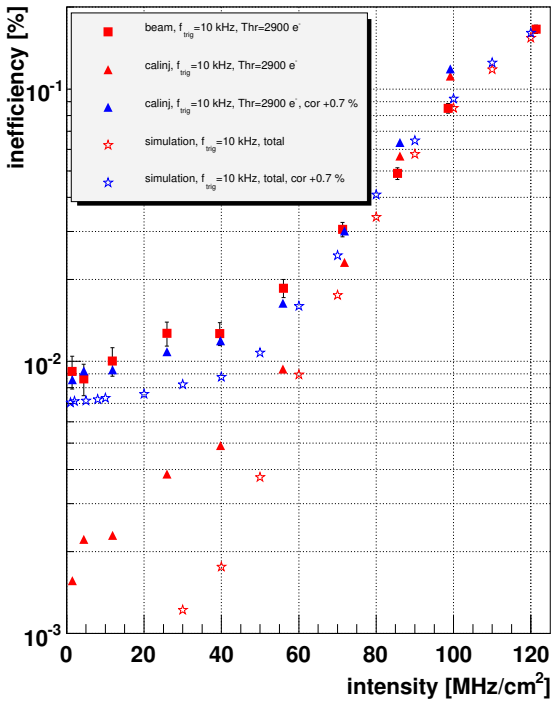

Figure 7.21: The inefficiencies versus the track densities for different trigger rates measured in the beam test. The corresponding results from the simulations and the measurements with calibrate signals are corrected with an additional inefficiency of 0.7 % (see text).

the values simulated for the CMS conditions are confirmed too. According to the Table 7.1 the inefficiency for the innermost layer under high luminosity operation with a L1T rate of 100 kHz results then in about 3.8 %.

7.8 Summary

A complete pixel detector module was operated under LHC like conditions in a high rate pion beam at PSI. No magnetic field was applied and the operating temperature was about 26 °C. The test module consisted of the final components. These are the readout chips PSI46V2, the Token Bit Manager TBM05 chip, the High Density Interconnect (HDI_V3), the final versions of the Kapton cable, the power cable and the base stripes.

The measured inefficiency is about 2 % for a track density of 60 MHz/cm^2 corresponding to the innermost layer of the pixel detector at high luminosity with a latency of 142 bunch crossings compared to 1 % resulting from the simulations. With additional inefficiencies not taken into account in the simulations like e.g. a sensor inefficiency of 0.5 % the measured data losses can be almost reproduced. Therefore the data losses seems to be described correctly in the simulation algorithm and applied to real CMS conditions an inefficiency of 3.8 % for the

innermost layer and a Level-1 Trigger rate of 100 kHz are expected.

The crosstalk measurements performed in the beam test confirmed the results from the laboratory measurements. The threshold shift caused by simultaneous readout operation and continuous data taking with beam is in the range of 300 electrons and therefore it is negligible compared to the global comparator threshold of 2500 electrons which is planned for CMS. The lowest global comparator threshold for a stable operation of the module in the beam test was about 2000 electrons.

With global delay scans appropriate values for the delays were found to operate the module with different bias voltages (70 V to 500 V) and various global comparator thresholds.

Chapter 8

Conclusions

In this work the design and the performance of the modules for the barrel of the CMS silicon pixel detector are described and test results are presented. The main contributions are beside the design of parts for the module the Single Event Upset (SEU) investigations, the intra module crosstalk measurements and the testing of the module performed in a LHC like high rate beam environment at PSI.

The most important components of a module are the 16 Readout Chips (ROCs) which are bump bonded to the silicon sensor. The control signals and the power are distributed on the module by a flexible, low mass printed circuit board. It is equipped with the Token Bit Manager (TBM) chip which organizes the readout of the 16 ROCs. The control signals are transmitted to the module by a Kapton cable and the power is provided by a laminated flat cable. For mechanical stability the structure is glued on two Si_3N_4 base stripes. The dimensions of the module are 66.6 mm $\times$ 26 mm. It is segmented into 66560 pixels and has a power consumption of about 2 W ($\sim$30 µW/pixel). The material budget of a module is without support and cooling structure about 1.2 % of one radiation length X_0 (1.6 % with mechanical support structure and coolant). The total weight is 2.2 g without cables and 3.5 g including both cables.

SEUs are a potential danger to loose some vital detector control functions. To investigate SEU effects test structures with shift registers consisting of standard Static Random Access Memory (SRAM) cells as used in the ROC with and without a protection capacitor were designed. Exposing the test structures and a ROC PSI46V1 to a particle beam the SEU cross sections of the SRAM cells were determined. The SEU cross sections are decreasing with an increasing supply voltage. The benefit of the protection capacitor is depending on the switching direction, but at least about a factor of 100 in the cross section. For the ROC the pion cross sections for the unprotected SRAM cells are 2.42×10^{-14} cm^2/SRAM for a transition from 0$\rightarrow$1 and 0.0115×10^{-14} cm^2/SRAM for a changeover from 1$\rightarrow$0. In the case of the protected SRAM cells the cross sections are 2.57×10^{-16} cm^2/SRAM for the switching direction 0$\rightarrow$1 and 0.529×10^{-16} cm^2/SRAM for changing the state from 1$\rightarrow$0. The impact of 300 MeV/c pions compared to 500 MeV/c protons is about a factor of 4.7 worse. With the measured cross sections the SEU rate per control network for the first and second layer is less than 0.03 Hz. In average it will take about 8 hours to switch 1‰ of all SRAM cells controlled by the corresponding digital optical link. This results in about 1 SEU per second for the entire pixel detector barrel ($\sim 48 \times 10^6$ pixels). Therefore reloading single pixel cells during

data taking period can be most likely avoided. For the final design of the ROC PSI46V2 the SRAM cells protected with an capacitor were used in the pixel unit cells and for the global digital analog converter registers.

A major requirement for the pixel detector is to perform continuous data taking and simultaneous readout operation with minimal dead-time and a maximum efficiency. To guaranty this the electronic crosstalk on the module must be as low as possible. Crosstalk for simultaneous column drains in large fractions of a module has been observed. During the start up of the column drain mechanism positive pickup was measured which caused a threshold shift for realistic cluster sizes in the range of about 40 electrons. The running column drain mechanism caused a negative pickup related to a threshold shift for realistic scenarios of about 200 electrons. For heavy ion collisions the threshold shift for starting up the column drain mechanism was estimated to be about 100 electrons and for the running column drain mechanism approximately 300 electrons. The readout of the 16 ROCs in a daisy chained way caused no observable crosstalk. Concerning a global threshold of 2500 electrons which is planned for the pixel detector the measured pickup caused by the column drain mechanism and the readout operation of the module is tolerable.

A pixel detector module was operated the first time under LHC like conditions in a high rate pion beam. No operational problem in the cooperation of the 16 ROCs with the TBM was observed under these conditions. The measured inefficiency for a track density of 62 MHz/cm^2 corresponding to LHC for the innermost layer of the pixel detector at high luminosity operation is at about 2 % compared to 1 % resulting from the simulations. With additional inefficiencies not taken into account in the simulations like e.g. a sensor inefficiency of 0.5 % the measured data losses can be almost reproduced. Therefore the data losses seem to be correctly described and applied to the real CMS conditions an inefficiency of 3.8 % for the innermost layer at a level-1 trigger rate of 100 kHz is expected. The crosstalk measurements performed in the beam test confirmed the results from the laboratory measurements. The threshold shift caused by simultaneous readout operation and continuous data taking with beam is in the range of 300 electrons and therefore it is acceptable compared to the global comparator threshold of 2500 electrons. The lowest global comparator threshold for a stable operation of the module in the beam test was about 2000 electrons. The module was operated with bias voltages up to 500 V.

Since the module performance fulfill the requirements the mass production of the modules has already started using the components with the final design described in this work. The goal of the production is to assembly and to test 4 modules per day. After the production of about 400 modules for the 4 cm and the 7 cm layer and the successful commissioning of the barrel part of the pixel vertex detector, the first data-taking is expected for late 2007.

Appendix A

SEU improved SRAM Memory Cell

In Figure A.1 a detailed schematic view of the unprotected (without protection capacitor; see Sect. 5.1) Static Random Access Memory (SRAM) cell as used in the Readout Chip (ROC) is shown. The drain and source implants of the nFETs are n^+-doped regions in the p-substrate. The substrate is on a potential close to V_{ss} (Sect.6.2). In the case of the pFETs the p^+-doped implants are sitting in a n^+-doped nwell with a potential close to V_{dd}. Therefore the implants of both types of transistors could form reverse biased p-n junctions with the substrate or the nwell depending on the potential at the contacts. Corresponding to the stored logic level in the SRAM cell the resulting reverse biased p-n junctions are indicated with colored circles and diode symbols in the Figure A.1.

In Section 5.1 it is explained that reverse biased p-n junctions are the most sensitive regions for SEUs. In the standard SRAM cell the number of reverse biased junctions is five independent of the logical level stored (HIGH≡1 or LOW≡0)). By exchanging the signal traces of Φ and $\bar{\Phi}$ with the traces connected to the output of the previous inverter the number of reverse biased junctions could be reduced from 5 to 3 (Fig. A.1 and Fig. A.2). The absolute number of p-n junctions is not relevant for the SEU sensitivity. However, the important value is the sensitive area which depends on the layout of the drain and source contacts of the FETs (ring transistors). Therefore the expected benefit of the reduction of the number of junctions from 5 to 3 is a factor of 4. This improvement should reduce the SEU rates in both flipping directions. These modifications of the SRAM cell will be implemented in the next ROC design.

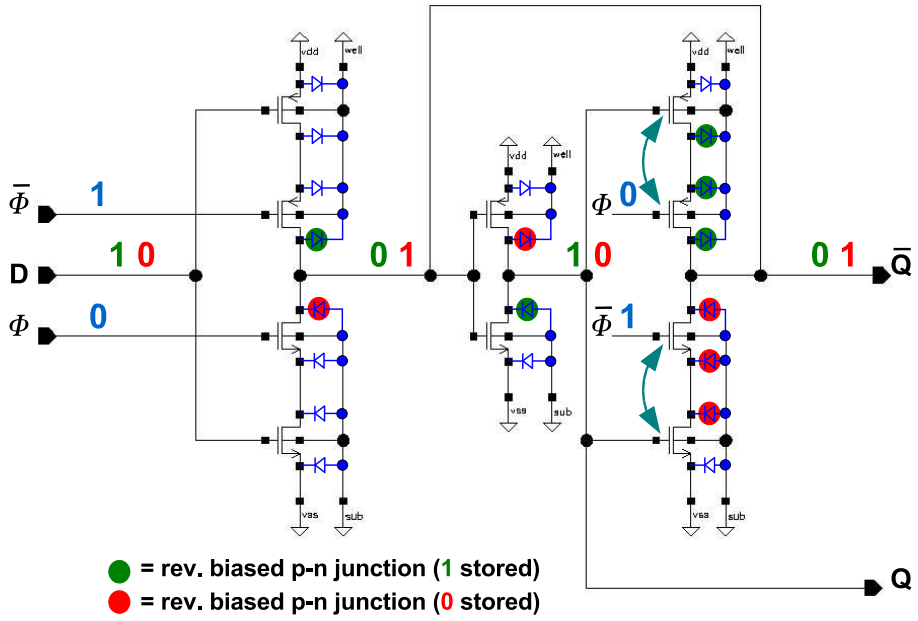

Figure A.1: Standard SRAM memory cell in the ROC PSI46V2. The five green and red circles mark the reverse biased p-n junctions (diode symbols) for the corresponding stored logic level in the cell. The arrows indicate the proposed changes to make the SRAM cell more resistant against a SEU.

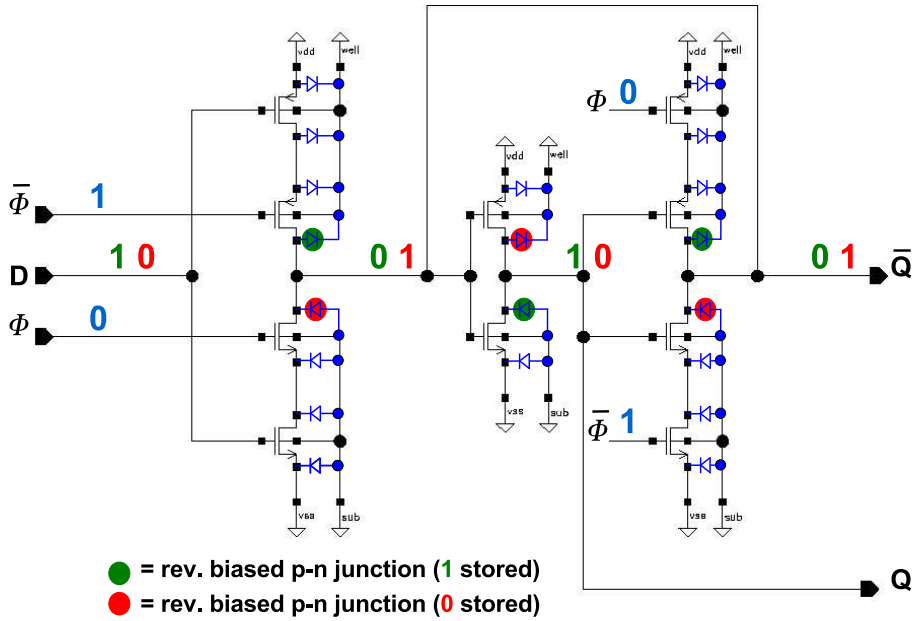

Figure A.2: SEU improved SRAM memory cell. The three green or red circles mark the reverse biased p-n junctions (diode symbols) for the corresponding stored logic level in the cell. The number of sensitive p-n junctions is reduced from 5 to 3 compared to the standard SRAM cell (Fig.A.1).

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